

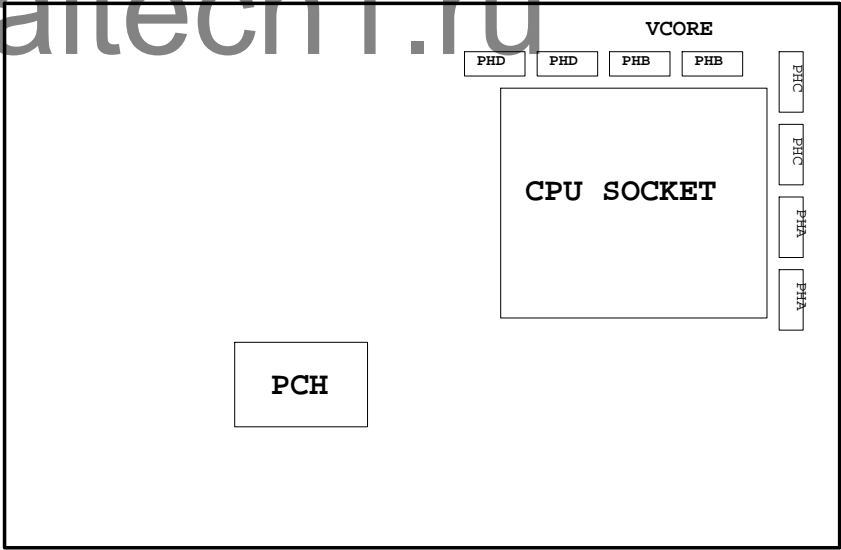
Model Name: GA-Z97X-UD3H

SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1150-A
05	CPU_LGA1150-B
06	CPU_LGA1150-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE
10	PCH_RGB,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCI EXPRESS*8 SLOT
16	PCI EXPRESS*16 SWITCH
17	PCI EXPRESS*4 SLOT
18	PCI EXPRESS*1 1,2,3 SLOT
19	ITE8892E
20	PCI SLOT
21	ALC1150 CODEC
22	REAR AUDIO JACK
23	ITE8620
24	COM/KB_MS/R_USB/PROHOT/USB PROTECT
25	ISL95820
26	ISL95820 VCORE Phase 8
27	DDR POWER

SHEET TITLE

28	DISCRETE POWER
29	DUAL BIOS
30	FP,F_USB,USB PWR,BZ
31	ATX POWER CONNECTOR
32	H/W MONITOR,FAN CTRL
33	DVI
34	HDMI_USB30
35	INTEL LAN I2I7
36	M.2_SATA_EXPRESS
37	TABLE LIST
39	
40	



MS

KB

RGB

DVI

USB3

USB3

HDMI

USB

USB

USB

USB

USB3

USB3

USB3

○

○

○

○

○

○

Gigabyte Technology

Title

Cover Sheet

Document Number

Z97X-UD3H

Date

Tuesday, April 08, 2014

Sheet

1

of

37

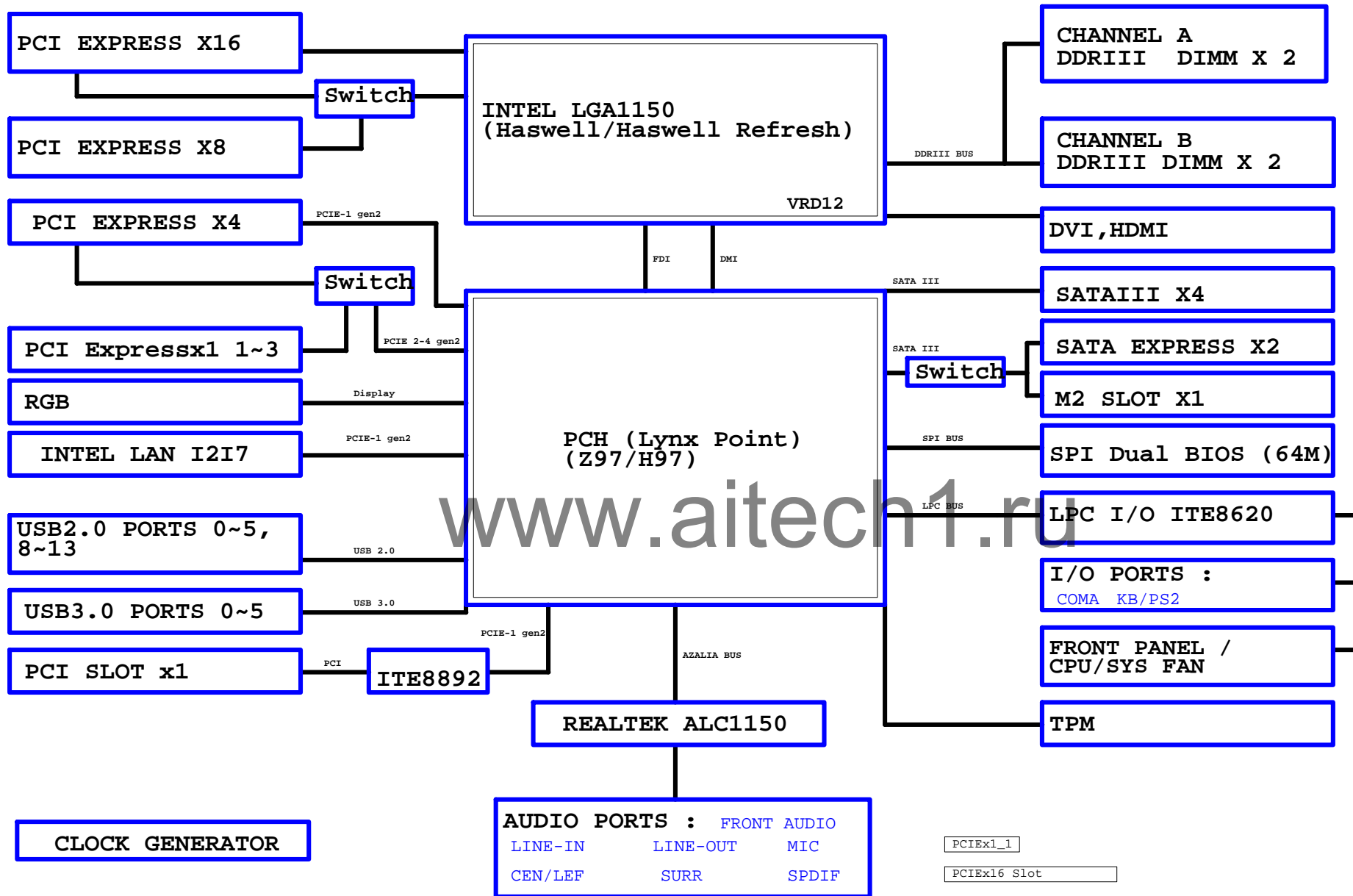
Rev

1.0

Component value change history

[illegible][illegible]

BLOCK DIAGRAM



- PCIEx1_1
- PCIEx16 Slot
- PCIEx1_2
- PCIEx1_3
- PCIEx8
- PCI Slot
- PCIEx4

LGA1150 (A)

LGA1150A									
	MAAA0	AU13	DDRO_MA0	DDRO_D00	A038	MDA0			
	MAAA1	AV16	DDRO_MA1	DDRO_D01	A039	MDA1			
	MAAA2	AU16	DDRO_MA2	DDRO_D02	AF38	MDA3			
	MAAA3	AU17	DDRO_MA3	DDRO_D03	AF39	MDA3			
	MAAA4	AU17	DDRO_MA4	DDRO_D03	A037	MDA4			
	MAAA5	AW18	DDRO_MA4	DDRO_D04	A040	MDA5			
	MAAA6	AV17	DDRO_MA5	DDRO_D05	AF37	MDA6			
	MAAA7	AT18	DDRO_MA6	DDRO_D06	AF40	MDA7			
	MAAA8	AW18	DDRO_MA7	DDRO_D07	AH40	MDA8			
	MAAA9	AT19	DDRO_MA8	DDRO_D08	AH39	MDA13			
	MAAA10	AW11	DDRO_MA9	DDRO_D09	AH38	MDA10			
	MAAA11	AV18	DDRO_MA10	DDRO_D10	AH39	MDA11			
	MAAA12	AU18	DDRO_MA11	DDRO_D11	AH37	MDA12			
	MAAA13	AX10	DDRO_MA12	DDRO_D12	AH38	MDA8			
	MAAA14	AT20	DDRO_M13	DDRO_D13	AH37	MDA14			
	MAAA15	AU21	DDRO_M14	DDRO_D14	AK40	MDA15			
			DDRO_M15	DDRO_D15	AM44	MDA17			
	MODT A0	AW10	DDRO_D16	DDRO_D16	AP39	MDA21			
	MODT A1	AY8	DDRO_OBT0	DDRO_D17	AP38	MDA18			
	MODT A2	AW9	DDRO_OBT1	DDRO_D18	AP39	MDA19			
	MODT A3	AU8	DDRO_OBT2	DDRO_D19	AP37	MDA20			
			DDRO_OBT3	DDRO_D20	AP38	MDA16			
				DDRO_D21	AP37	MDA22			
		AW33	DDRO_D22	DDRO_D22	AP40	MDA23			
		AX33	DDRO_ECC0	DDRO_D23	AV37	MDA25			
		AU31	DDRO_ECC1	DDRO_D24	AW37	MDA29			
		AX31	DDRO_ECC2	DDRO_D25	AU35	MDA26			
		AT33	DDRO_ECC3	DDRO_D26	AV35	MDA27			
		AT31	DDRO_ECC4	DDRO_D27	AT37	MDA28			
		AX31	DDRO_ECC5	DDRO_D28	AU37	MDA24			
		AW31	DDRO_ECC6	DDRO_D29	AT35	MDA30			
			DDRO_ECC7	DDRO_D30	AW35	MDA31			
				DDRO_D31	AY6	MDA33			
	SBA0	SBA0	DDRO_BA0	DDRO_D32	AU6	MDA37			
7	SBA1	SBA1	DDRO_BA1	DDRO_D33	AY4	MDA34			
7	SBA2	SBA2	DDRO_BA2	DDRO_D34	AY4	MDA35			
				DDRO_D35	AW6	MDA36			
	CKE0	CKE0	DDRO_CK0	DDRO_D36	AW8	MDA32			
7	CKE1	CKE1	DDRO_CK1	DDRO_D37	AW4	MDA38			
7	CKE2	CKE2	DDRO_CK2	DDRO_D38	AW4	MDA39			
7	CKE3	CKE3	DDRO_CK3	DDRO_D39	AR1	MDA41			
				DDRO_D40	AN3	MDA45			
	-CSA0	-CSA0	DDRO_CS_N0	DDRO_D41	AN3	MDA47			
7	-CSA1	-CSA1	DDRO_CS_N1	DDRO_D42	AN4	MDA43			
7	-CSA2	-CSA2	DDRO_CS_N2	DDRO_D43	AR3	MDA44			
7	-CSA3	-CSA3	DDRO_CS_N3	DDRO_D44	AR2	MDA40			
				DDRO_D45	AN1	MDA46			
7	DCLKA0	DCLKA0	DDRO_CLK_P0	DDRO_D46	AN1	MDA47			
7	DCLKA0	DCLKA0	DDRO_CLK_P0	DDRO_D47	AL1	MDA49			
7	DCLKA1	DCLKA1	DDRO_CLK_P1	DDRO_D48	AJ4	MDA53			
7	DCLKA1	DCLKA1	DDRO_CLK_P1	DDRO_D49	AL3	MDA50			
7	DCLKA2	DCLKA2	DDRO_CLK_P2	DDRO_D50	AJ4	MDA51			
7	DCLKA2	DCLKA2	DDRO_CLK_P2	DDRO_D51	AJ2	MDA52			
7	DCLKA3	DCLKA3	DDRO_CLK_P3	DDRO_D52	AJ4	MDA48			
7	DCLKA3	DCLKA3	DDRO_CLK_P3	DDRO_D53	AJ7	MDA54			
		AX12	RSVD	DDRO_D54	D11	MDA55			
				DDRO_D55	AG1	MDA57			
				DDRO_D56	MDA61				
				DDRO_D57	AG4	MDA58			
				DDRO_D58	AE3	MDA59			
				DDRO_D59	AG2	MDA60			
				DDRO_D60	AG3	MDA56			
				DDRO_D61	AG3	MDA62			
				DDRO_D62	AE1	MDA63			
7	-SRASA	-SRASA	DDRO_RAS*	DDRO_D63	AE39	DSOA50			
				DDRO_D64	AN39	DSOA1			
	-SWEA	-SWEA	DDRO_WE*	DDRO_DOS_P0	AV38	DSOA2			
				DDRO_DOS_P1	AV35	DSOA3			
		AV20	RSVD	DDRO_DOS_P2	AF3	DSOA4			
		AX27	RSVD	DDRO_DOS_P3	AF3	DSOA5			
				DDRO_DOS_P4	AF3	DSOA6			
				DDRO_DOS_P5	AF3	DSOA7			
7	-SCASA	-SCASA	DDRO_CAS*	DDRO_DOS_P6	AK3	DSOA8			
		AU9		DDRO_DOS_P7	AJ3	DSOA9			
7,8	-DDR3_RST	WR61 MASK/U4/SH/TX WC4 0.1uA/IX7R16V/IX N3	DDR_RESET*	DDRO_DOS_P8	AV32	DSOA0			
				DDRO_DOS_P9	AE38	DSOA1			
				DDRO_DOS_N1	AN38	DSOA2			
				DDRO_DOS_N2	AU36	DSOA3			
				DDRO_DOS_N3	AW5	DSOA4			
				DDRO_DOS_N4	AP2	DSOA5			
				DDRO_DOS_N5	AK2	DSOA6			
				DDRO_DOS_N6	AE2	DSOA7			
				DDRO_DOS_N7	AU32				
				DDRO_DOS_N8					

HASWELL/[10SC1-F01150-01R_10SC1-F01150-03R]

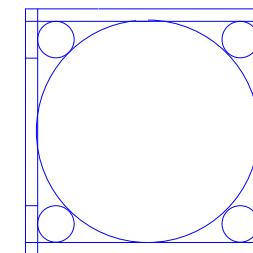
LGA1150 (B)

		LGA150B			
MAAB0	AL19	DDR1_MA0	DDR1_D00	A634	MD80
MAAB1	AK23	DDR1_MA1	DDR1_D01	A635	MD81
MAAB2	AM22	DDR1_MA2	DDR1_D02	AG35	MD82
MAAB3	AM23	DDR1_MA3	DDR1_D03	AH35	MD83
MAAB4	AP23	DDR1_MA4	DDR1_D04	AD34	MD84
MAAB5	AL23	DDR1_MA5	DDR1_D05	AD55	MD85
MAAB6	AY24	DDR1_MA6	DDR1_D06	AG34	MD86
MAAB7	AZ24	DDR1_MA7	DDR1_D07	AH34	MD87
MAAB8	AW25	DDR1_MA8	DDR1_D08	AL34	MD88
MAAB9	AW25	DDR1_MA9	DDR1_D09	AL35	MD89
MAAB10	AP18	DDR1_MA10	DDR1_D10	AK31	MD10
MAAB11	AY25	DDR1_MA11	DDR1_D011	AL31	MD11
MAAB12	AZ26	DDR1_MA12	DDR1_D012	AK34	MD12
MAAB13	AR15	DDR1_MA13	DDR1_D013	AK35	MD13
MAAB14	AV27	DDR1_MA14	DDR1_D014	AK32	MD14
MAAB15	AW28	DDR1_MA15	DDR1_D015	AL32	MD15
MODT_B0	AM17	DDR1_ODT0	DDR1_D016	AN34	MD17
MODT_B1	AL16	DDR1_ODT1	DDR1_D017	AP34	MD21
MODT_B2	AM16	DDR1_ODT19	DDR1_D018	AN31	MD19
MODT_B3	AK15	DDR1_ODT3	DDR1_D020	AP31	MD23
			DDR1_D021	AN35	MD20
			DDR1_D022	AP35	MD16
			DDR1_D023	AN32	MD18
	AM26	DDR1_ECC0	DDR1_D024	AP29	MD22
	AM25	DDR1_ECC1	DDR1_D025	AM29	MD25
	AP25	DDR1_ECC2	DDR1_D026	AM28	MD28
	AL26	DDR1_ECC3	DDR1_D028	AR29	MD27
	AL26	DDR1_ECC4	DDR1_D028	AR28	MD30
	AR26	DDR1_ECC5	DDR1_D027	AL29	MD24
	AR26	DDR1_ECC6	DDR1_D028	AL28	MD29
	AR25	DDR1_ECC7	DDR1_D029	AP29	MD36
			DDR1_D030	AP28	MD31
SBAB0	AK17	DDR1_BA0	DDR1_D031	AR12	MD32
SBAB1	AL18	DDR1_BA1	DDR1_D032	AP12	MD33
SBAB2	AW28	DDR1_BA2	DDR1_D033	AL13	MD35
			DDR1_D034	AL12	MD36
CKEB0	AW29	DDR1_CKE0	DDR1_D038	AR13	MD36
CKEB1	AZ29	DDR1_CKE1	DDR1_D036	AP13	MD37
CKEB2	AU28	DDR1_CKE2	DDR1_D037	AM13	MD38
CKEB3	AU29	DDR1_CKE3	DDR1_D038	AM12	MD39
			DDR1_D039	AR9	MD45
CSB0	AP17	DDR1_CS_N0	DDR1_D040	AP9	MD41
CSB1	AN15	DDR1_CS_N1	DDR1_D041	AR6	MD47
CSB2	AN17	DDR1_CS_N2	DDR1_D042	AP6	MD44
CSB3	AL15	DDR1_CS_N3	DDR1_D043	AR10	MD44
			DDR1_D044	AP10	MD46
			DDR1_D045	AR7	MD40
DLCKB0	AM20	DDR1_DLK_P0	DDR1_D047	AP7	MD42
DLCKB1	AP21	DDR1_DLK_N0	DDR1_D048	AL9	MD52
DLCKB2	AP22	DDR1_DLK_N1	DDR1_D051	AL6	MD60
DLCKB3	AN21	DDR1_DLK_P2	DDR1_D051	AM10	MD49
DLCKB4	AN20	DDR1_DLK_N2	DDR1_D052	AL10	MD49
DLCKB5	AP19	DDR1_DLK_P3	DDR1_D053	AM6	MD54
DLCKB6	AP20	DDR1_DLK_N3	DDR1_D055	AM7	MD51
DLCKB7	AP18	DDR1_DLK_P4	DDR1_D056	AH6	MD61
DLCKB8	AP17	DDR1_DLK_P5	DDR1_D057	AH7	MD60
DLCKB9	AP16	DDR1_DLK_P6	DDR1_D057	A66	MD59
DLCKB10	AL20	DDR1_DLK_P7	DDR1_D058	A67	MD63
DLCKB11	AM18	DDR1_RAS*	DDR1_D060	AJ6	MD56
DLCKB12	AK16	DDR1_RAS*	DDR1_D061	AJ7	MD57
DLCKB13		DDR1_WE*	DDR1_D062	A66	MD58
DLCKB14			DDR1_D063	A67	MD62
DLCKB15			DDR1_D064	AF35	MD80
DLCKB16			DDR1_D065	AF33	MD81</

HASWELL/[10SC1-F01150-01R_10SC1-F01150-03R]

LGA1150 (CR)

LGA1150
ILM_BP_CR/115X/BKNI/[12KRC-0F0001-61R_12KRC-0F0001-62R]



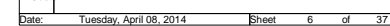
DDR BUS

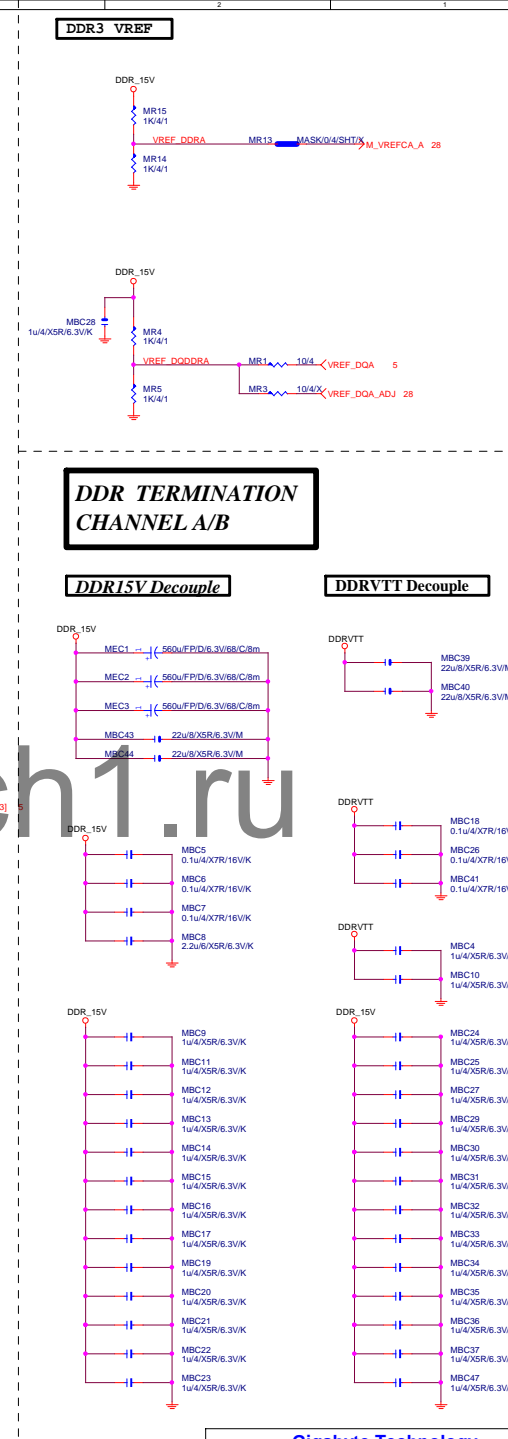
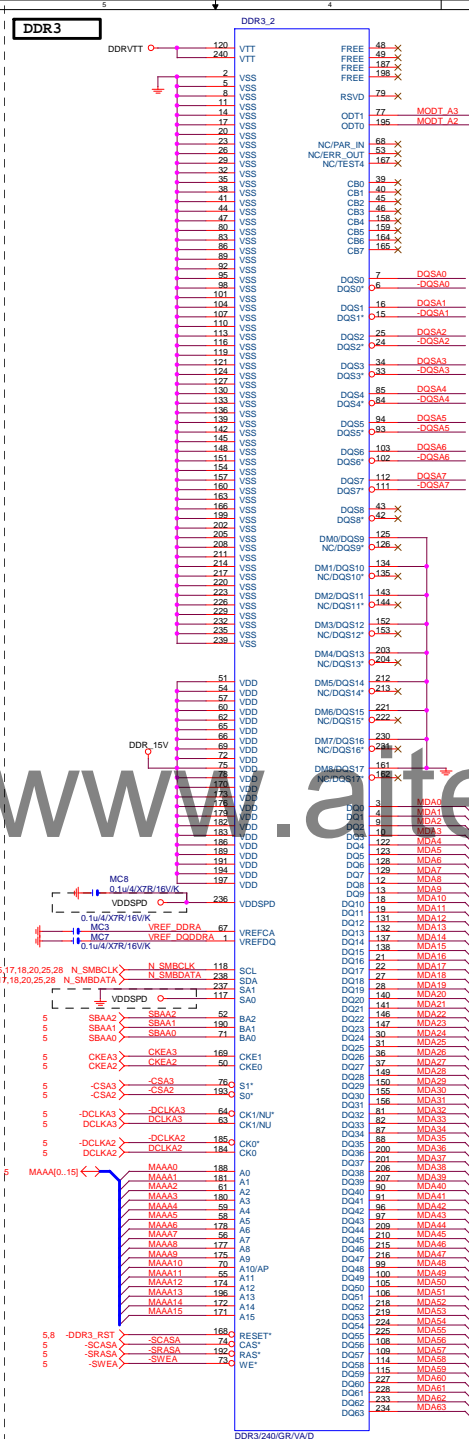
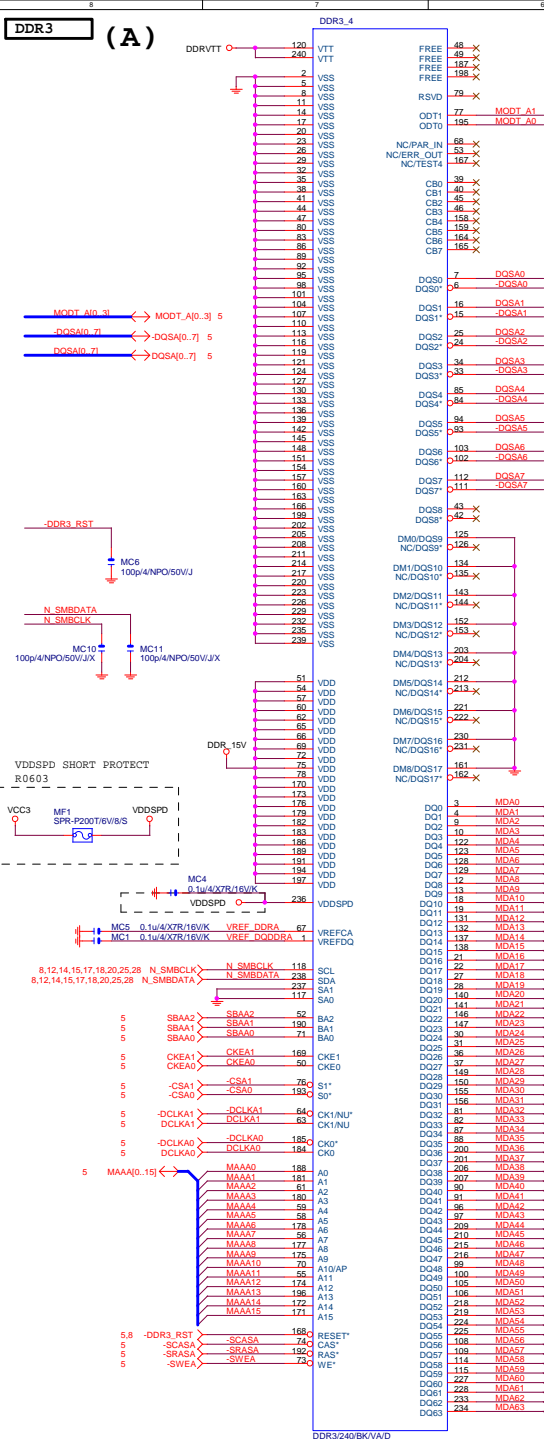
7	MODT_A[0..3]	↔	MODT_AIO_3
8	MODT_B[0..3]	↔	MODT_BIO_3
7	MDA[0..63]	↔	MDAIO_63
8	MDB[0..63]	↔	MDBIO_63
7	DQSA[0..7]	↔	DQSAIO_7
7	-DQSA[0..7]	↔	-DQSAIO_7
7	MAAA[0..15]	↔	MAAAIO_15
8	MAAB[0..15]	↔	MAABIO_15
8	DQSB[0..7]	↔	DQSBIO_7
8	-DQSB[0..7]	↔	-DQSBIO_7

Gigabyte Technology

Title				CPU LGA1150-B			
Size	Custom	Document Number				Rev	
		Z97X-UD3H				1.0	
Date:		Tuesday, April 08, 2014		Sheet		5 of 37	

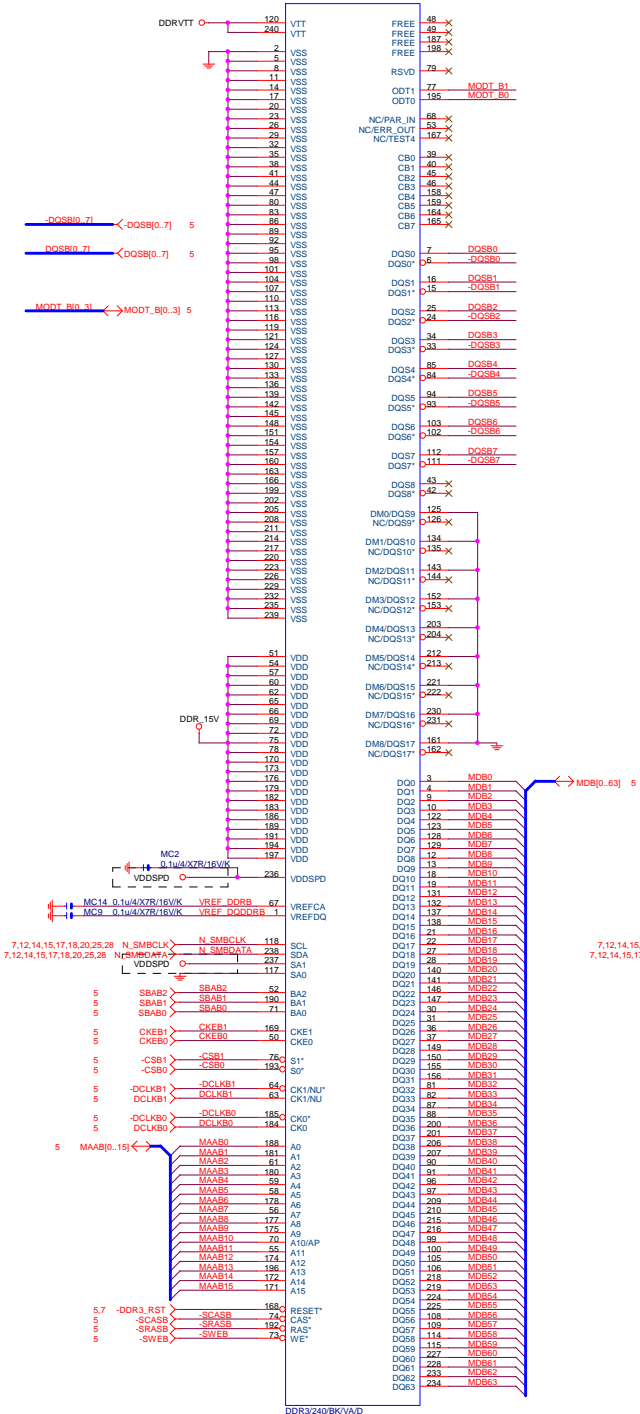
(F, J)



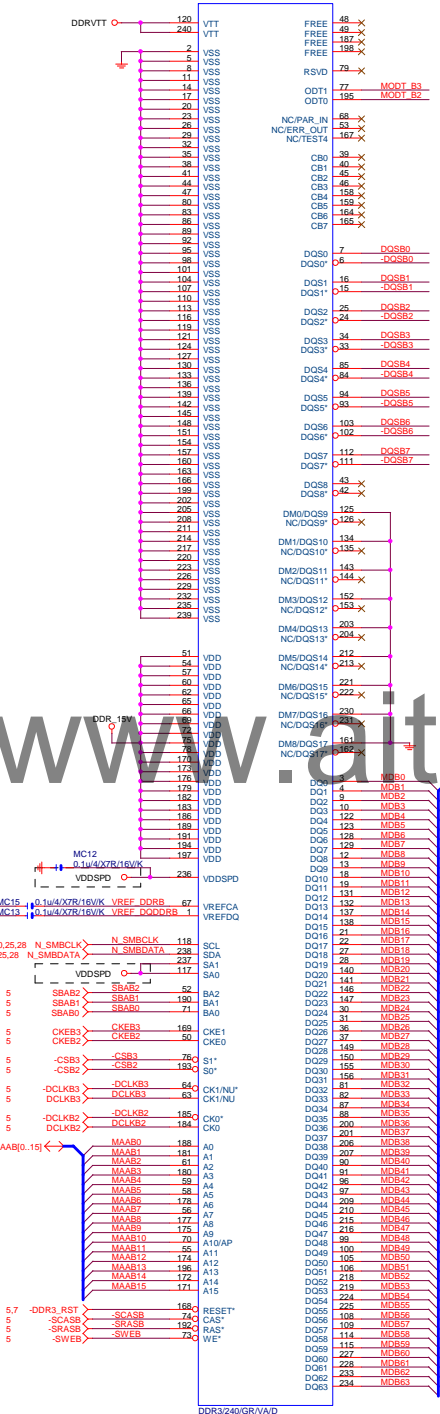


DDR3

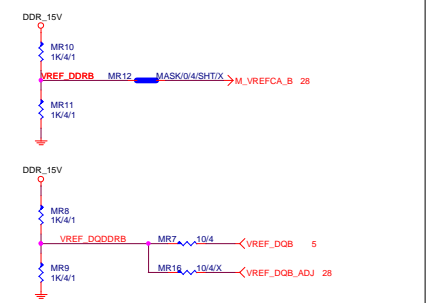
(B)



DDR3



DDR3 VREF



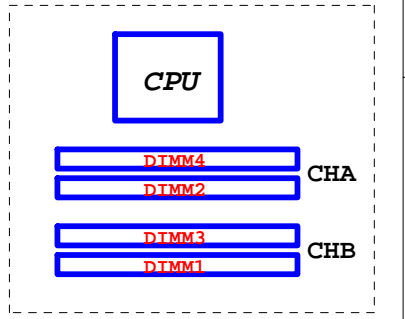
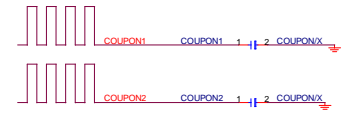
DDR3 1066,1333,1600MHZ BANDWIDTH

DDR3 1066MHZ
DDR3 clock=533MHZ
DDR3 single channel bandwidth=533x2x8Byte=8.5GB/s
DDR3 dual channel bandwidth=533x2x2x8Byte=17GB/s

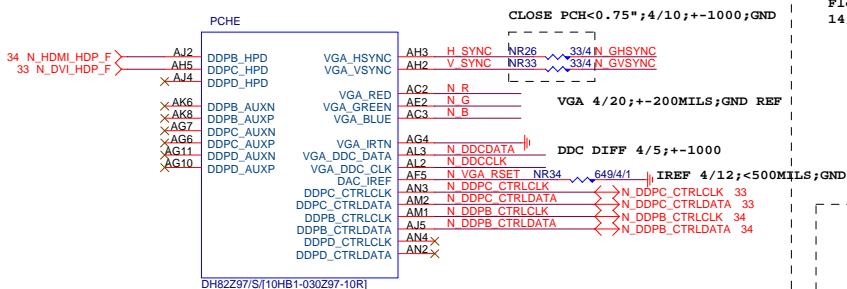
DDR3 1333MHZ
DDR3 clock=667MHZ
DDR3 single channel bandwidth=10.6GB/s
DDR3 dual channel bandwidth=21GB/s

DDR3 1600MHZ
DDR3 clock=800MHZ
DDR3 single channel bandwidth=12.8GB/s
DDR3 dual channel bandwidth=25.6GB/s

COUPON

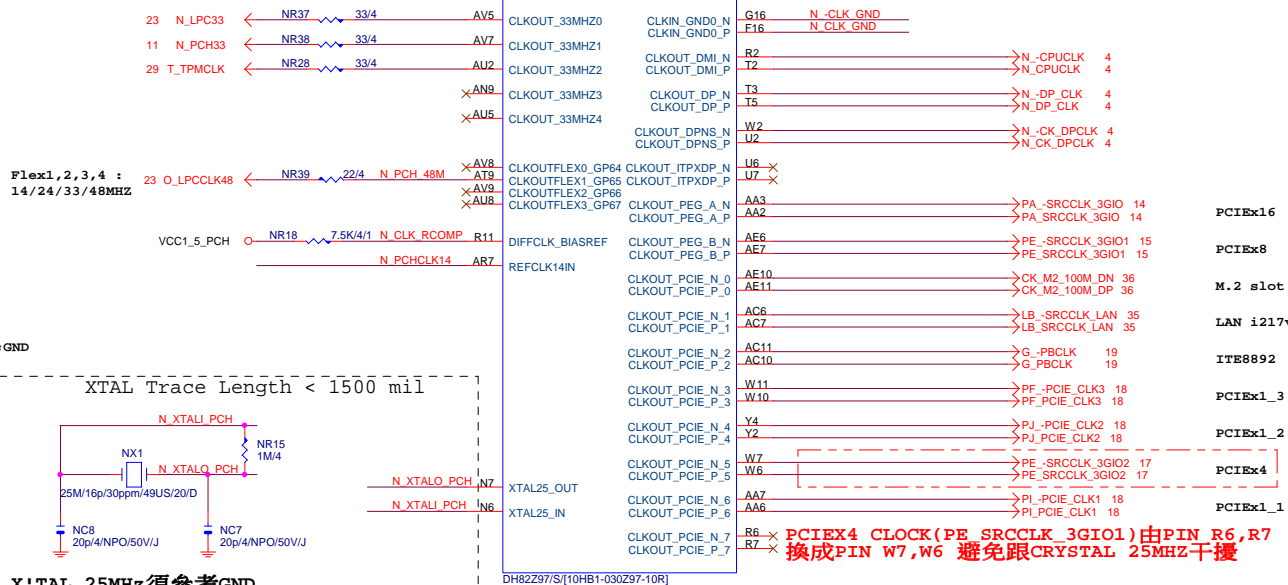


PCH (E)



VGA_DISABLE
R,G,B NC OR GND
IRTN / IREF GND
VGA_HSYNC, VGA_VSYNC, DDC_CLK, DDC_DATA NC
POWER VCCADAC(AF2), VCCADACBG(AE1) GND

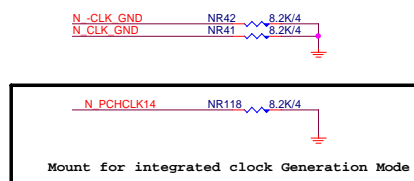
PCH (G)



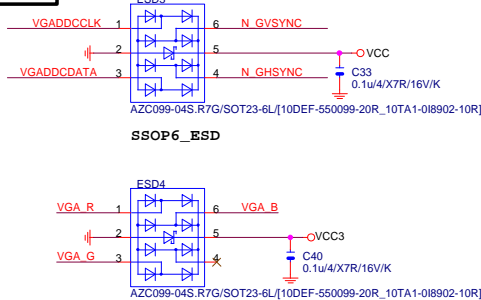
M2 Clock需接Clock#0

Differential Clock:18/4/6/4/18
Impedance=90 +- 15%

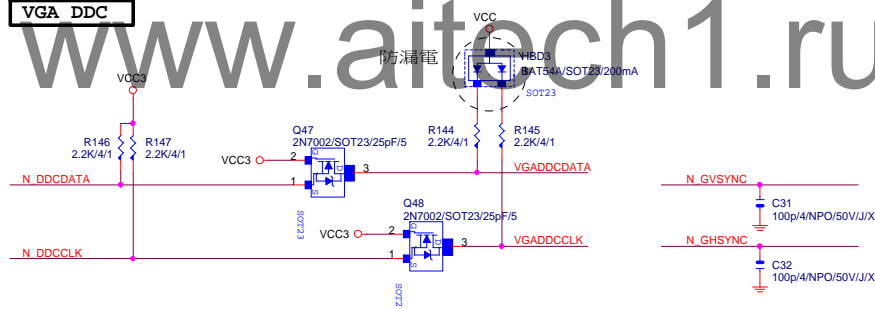
PCH CLK PD



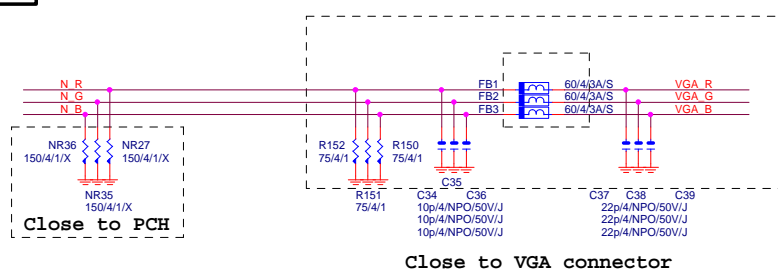
VGA ESD



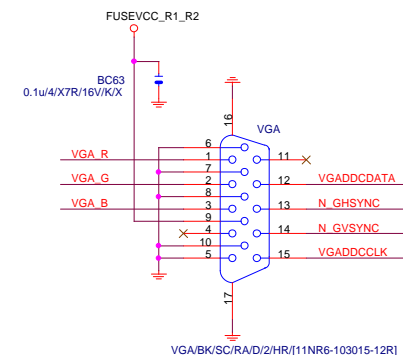
VGA DDC



VGA DDC



VGA CONNECTOR



Gigabyte Technology

Title			
PCH DISPLAY ,CLK BUFFER			
Size	Document Number	Rev	
Custom	Z97X-UD3H	1.0	
Date:	Tuesday, April 08, 2014	Sheet	10 of 37

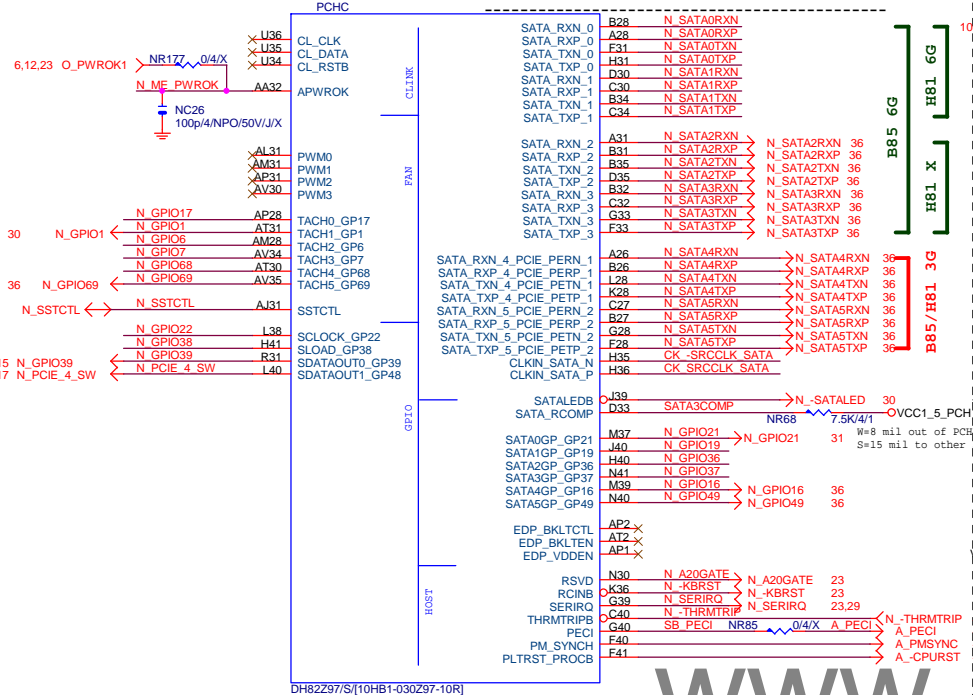
PCH (C)

SATA3 : 20/4/4/4/20 (breakout min 8/4/4/4/8)
Impedance=85 \pm 17.5%

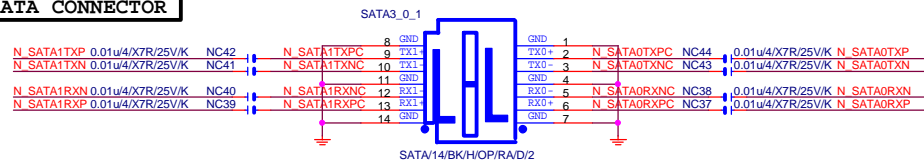
Impedance=85

SATA2 4/4/4//15

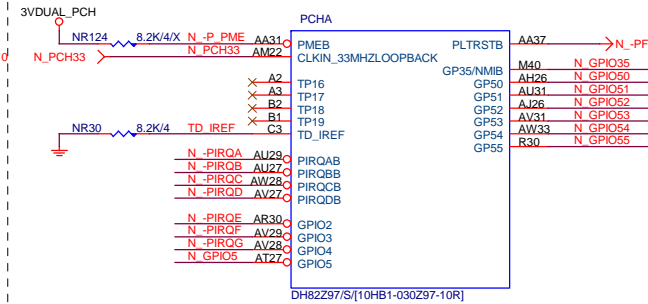
SATA3 4/4/4//20



SATA CONNECTOR



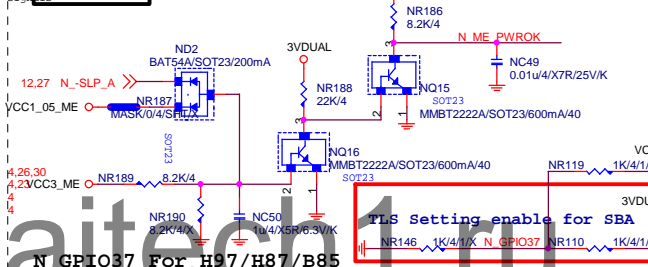
PCH (A)



```
Default int pull up on GP51,
Default SPI boot devices
```

BOOT DEVICE	GP51	GP19
LPC	0	0
SPI	float	float

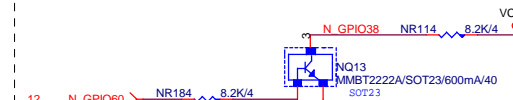
ME PWROK



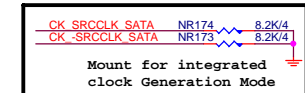
GPIO38 Ctrl

MFG Mode

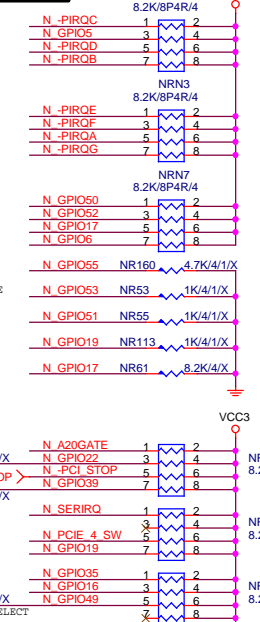
```
N_GPIO38 : Lo --> Enable
           Hi --> Disable
```



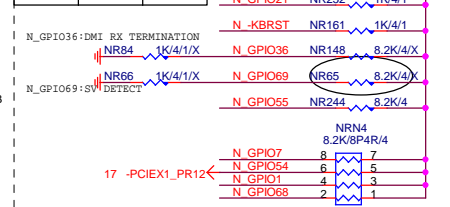
PCH CLK PD



PCH PU/PD



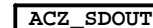
soft strap	GP16	GP49
0	pcie1	pcie2
1	sata4	sata5



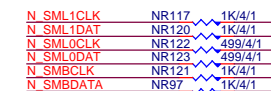
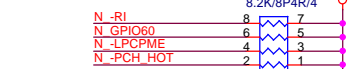
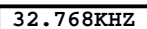
Gigabyte Technology

Title			
PCH HOST , SATA, PCI			
Size	Document Number		Rev
Custom	Z97X-UD3H		1.0
Date:	Tuesday, April 08, 2014	Sheet	11 of 37

(D)



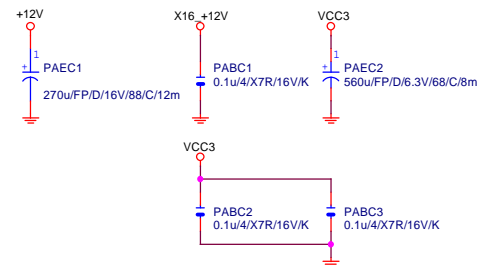
PCH	PU/PD
-----	-------



Gigabyte Technology

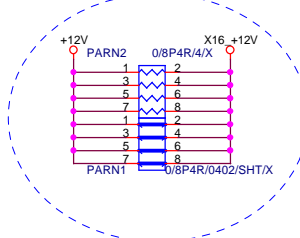
Title			
PCH GPIO , CTRL , AUDIO			
Size	Document Number	Rev	
Custom	Z97X-UD3H	1.0	
Date:	Tuesday, April 08, 2014	Sheet	12 of 37

PCIEX16 CAP



PCIEX16 PROTECT SHT

+12 protect short-wire test



PCIEX16 AC CAP

PA EXP TXP0	PAC5	0.22u/4/X5R/6.3V/K	PA EXP TXP0 C
PA EXP TXN0	PAC4	0.22u/4/X5R/6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PAC6	0.22u/4/X5R/6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PAC7	0.22u/4/X5R/6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PAC8	0.22u/4/X5R/6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u/4/X5R/6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u/4/X5R/6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u/4/X5R/6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u/4/X5R/6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u/4/X5R/6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u/4/X5R/6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u/4/X5R/6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u/4/X5R/6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u/4/X5R/6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PAC18	0.22u/4/X5R/6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PAC19	0.22u/4/X5R/6.3V/K	PA EXP TXN7 C
PA EXP SW TXP8	PAC20	0.22u/4/X5R/6.3V/K	PA EXP SW TXP8 C
PA EXP SW TXN8	PAC21	0.22u/4/X5R/6.3V/K	PA EXP SW TXN8 C
PA EXP SW TXP9	PAC22	0.22u/4/X5R/6.3V/K	PA EXP SW TXP9 C
PA EXP SW TXN9	PAC23	0.22u/4/X5R/6.3V/K	PA EXP SW TXN9 C
PA EXP SW TXP10	PAC24	0.22u/4/X5R/6.3V/K	PA EXP SW TXP10 C
PA EXP SW TXN10	PAC25	0.22u/4/X5R/6.3V/K	PA EXP SW TXN10 C
PA EXP SW TXP11	PAC26	0.22u/4/X5R/6.3V/K	PA EXP SW TXP11 C
PA EXP SW TXN11	PAC27	0.22u/4/X5R/6.3V/K	PA EXP SW TXN11 C
PA EXP SW TXP12	PAC28	0.22u/4/X5R/6.3V/K	PA EXP SW TXP12 C
PA EXP SW TXN12	PAC29	0.22u/4/X5R/6.3V/K	PA EXP SW TXN12 C
PA EXP SW TXP13	PAC30	0.22u/4/X5R/6.3V/K	PA EXP SW TXP13 C
PA EXP SW TXN13	PAC31	0.22u/4/X5R/6.3V/K	PA EXP SW TXN13 C
PA EXP SW TXP14	PAC32	0.22u/4/X5R/6.3V/K	PA EXP SW TXP14 C
PA EXP SW TXN14	PAC33	0.22u/4/X5R/6.3V/K	PA EXP SW TXN14 C
PA EXP SW TXP15	PAC34	0.22u/4/X5R/6.3V/K	PA EXP SW TXP15 C
PA EXP SW TXN15	PAC35	0.22u/4/X5R/6.3V/K	PA EXP SW TXN15 C

PCI-E REV:1.1--> 2.5GHZ

PCE-E X1(單向) BANDWITH=2.5GHZ*(8b/10b)=2Gb/s=250MB/s

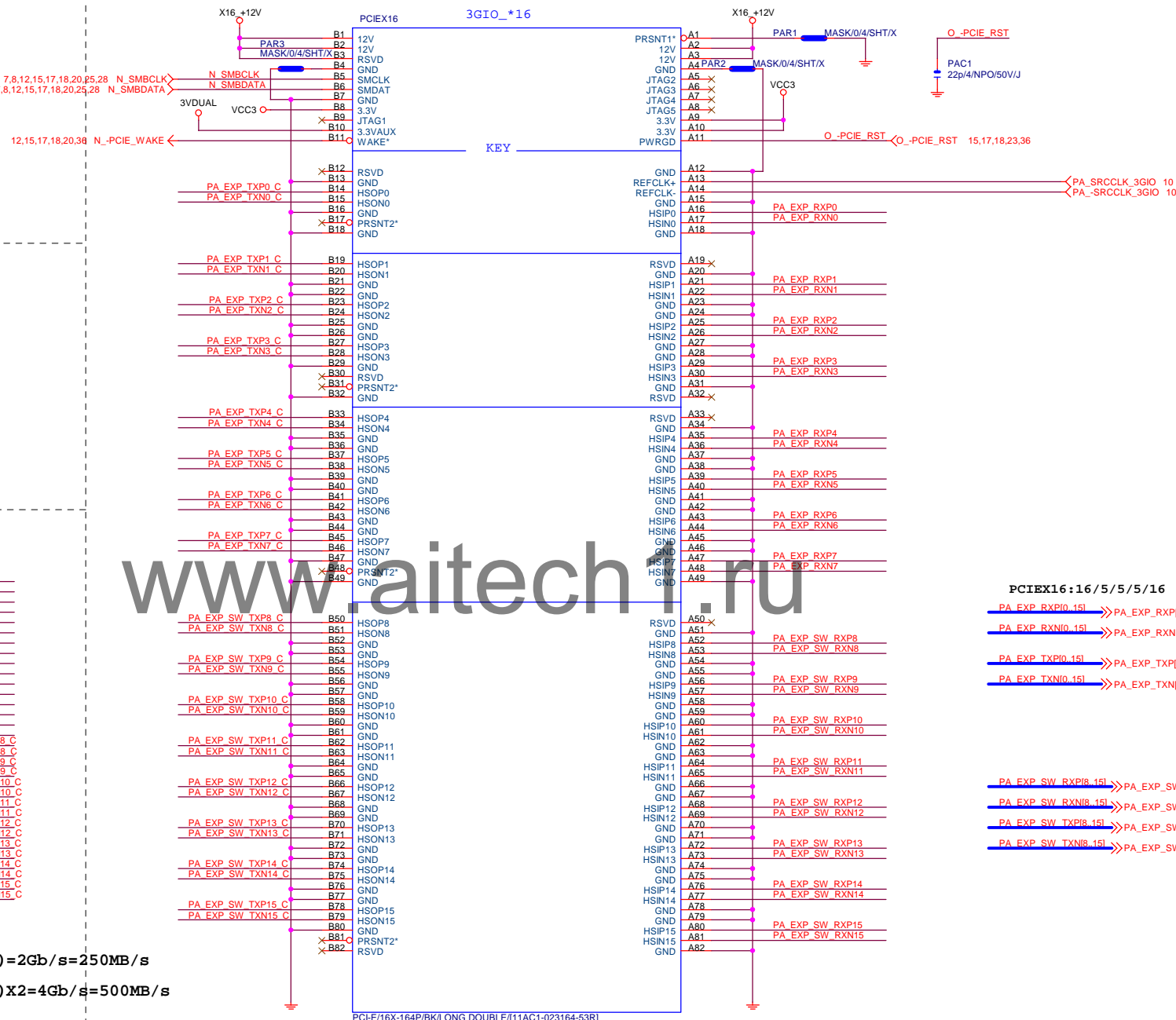
PCE-E X1(雙向) BANDWITH=2.5GHZ*(8b/10b)X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWITH=2.5GHZ*(8b/10b)X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWITH=2.5GHZ*(8b/10b)X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHZ

PCIEX16 SLOT



PCIEX16:16/5/5/5/16

PA EXP RXP0.15] >>> PA_EXP_RXP0[0..15] 4,16

PA EXP RXN0.15] >>> PA_EXP_RXN0[0..15] 4,16

PA EXP TXP0.15] >>> PA_EXP_TXP0[0..15] 4,16

PA EXP TXN0.15] >>> PA_EXP_TXN0[0..15] 4,16

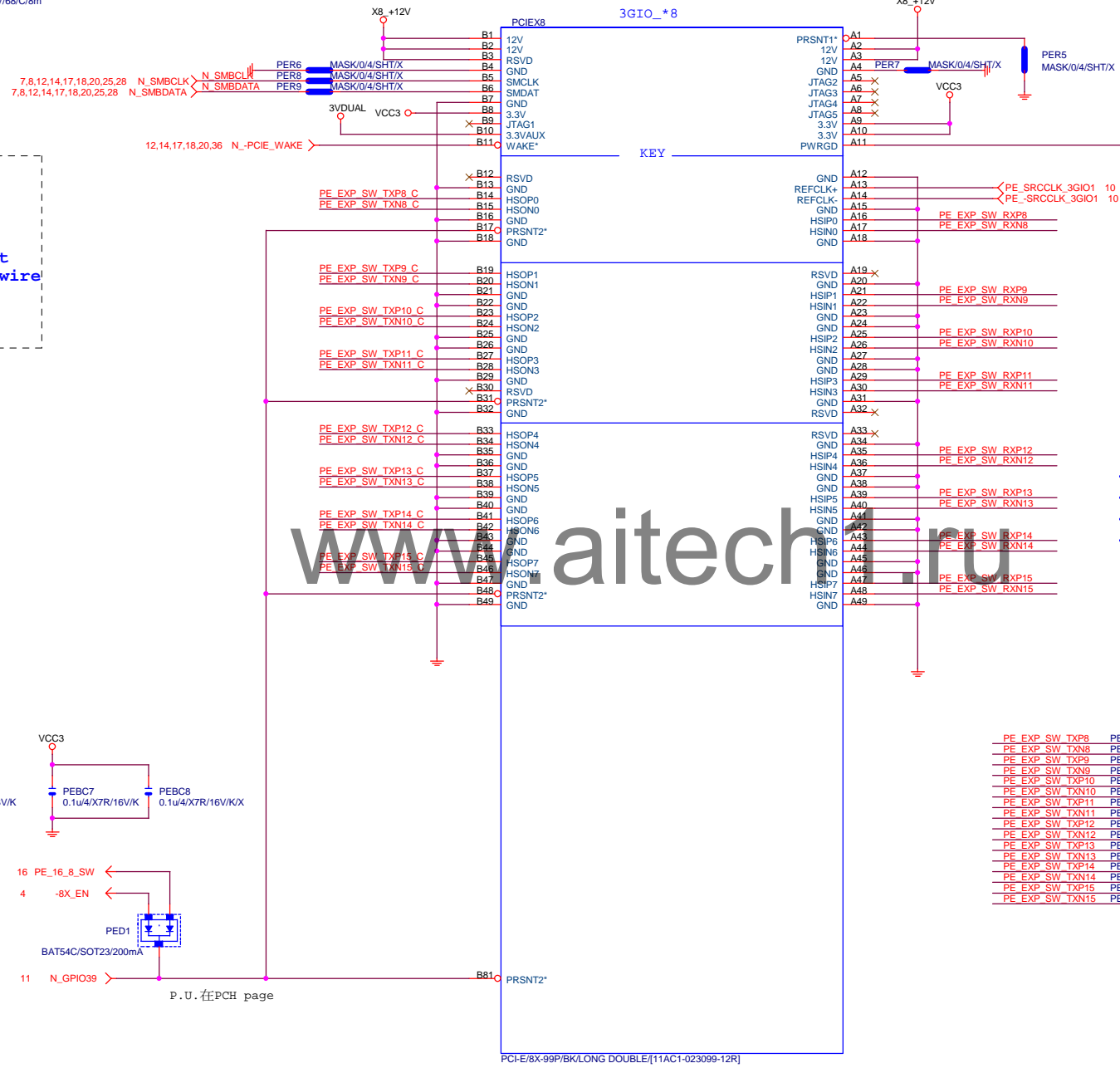
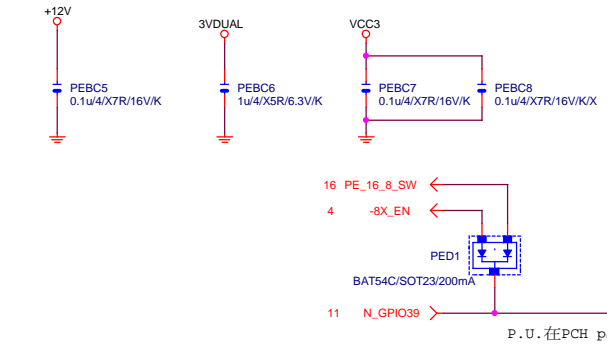
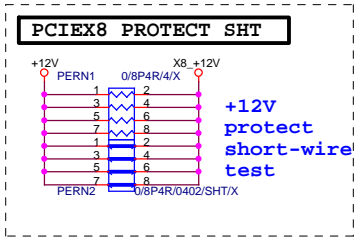
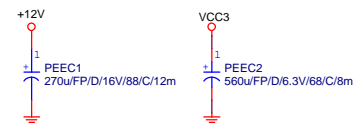
PA EXP SW RXP8.15] >>> PA_EXP_SW_RXP8[8..15] 16

PA EXP SW RXN8.15] >>> PA_EXP_SW_RXN8[8..15] 16

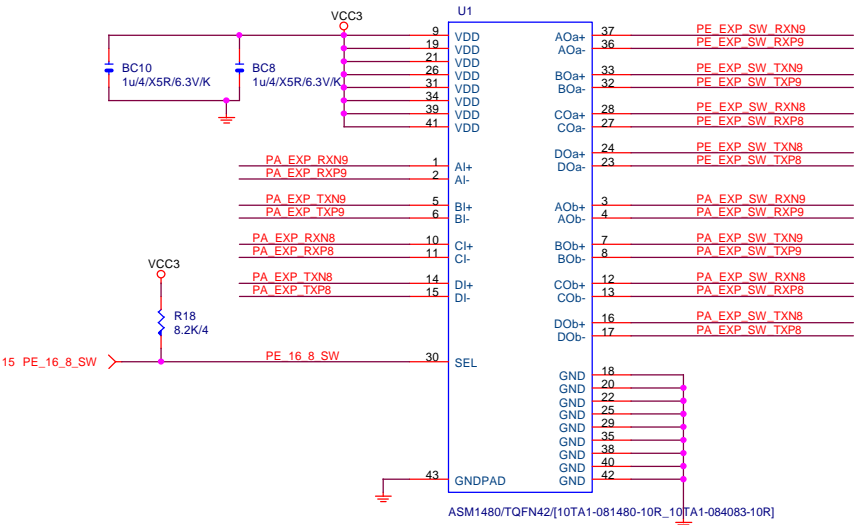
PA EXP SW TXP8.15] >>> PA_EXP_SW_TXP8[8..15] 16

PA EXP SW TXN8.15] >>> PA_EXP_SW_TXN8[8..15] 16

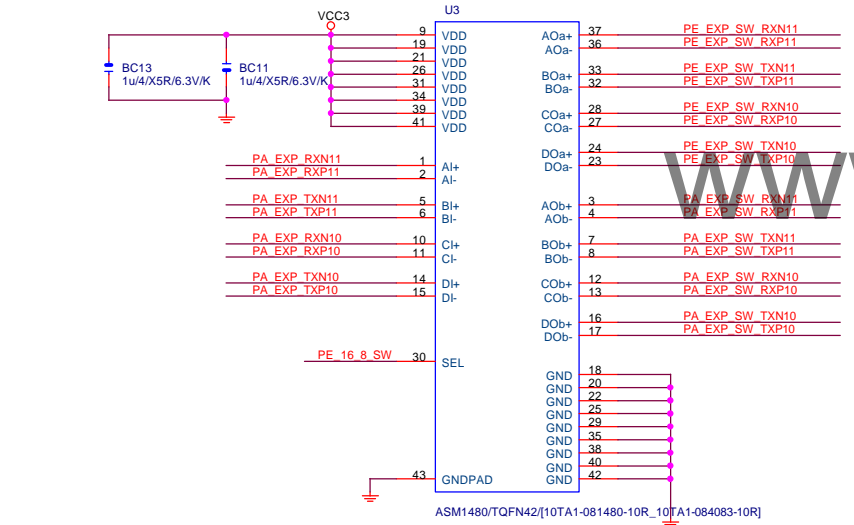
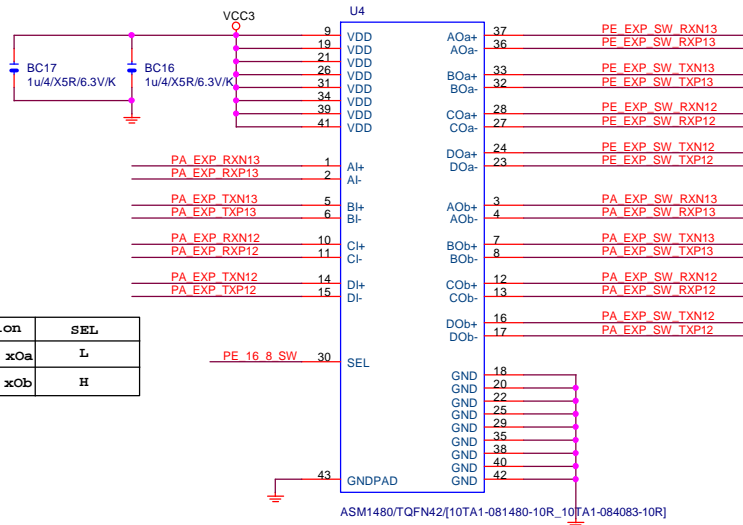
Gigabyte Technology			
PCI EXPRESS * 16			
Title	Document Number	Rev	
	297X-UD3H	1.0	
Date:	Tuesday, April 08, 2014	Sheet	14 of 37



PE EXP SW TXP8	PEC7	0.22u4/X5R/6.3V/K	PE EXP SW TXP8_C
PE EXP SW TXN8	PEC8	0.22u4/X5R/6.3V/K	PE EXP SW TXN8_C
PE EXP SW TXP9	PEC9	0.22u4/X5R/6.3V/K	PE EXP SW TXP9_C
PE EXP SW TXN9	PEC10	0.22u4/X5R/6.3V/K	PE EXP SW TXN9_C
PE EXP SW TXP10	PEC11	0.22u4/X5R/6.3V/K	PE EXP SW TXP10_C
PE EXP SW TXN10	PEC12	0.22u4/X5R/6.3V/K	PE EXP SW TXN10_C
PE EXP SW TXP11	PEC13	0.22u4/X5R/6.3V/K	PE EXP SW TXP11_C
PE EXP SW TXN11	PEC14	0.22u4/X5R/6.3V/K	PE EXP SW TXN11_C
PE EXP SW TXP12	PEC15	0.22u4/X5R/6.3V/K	PE EXP SW TXP12_C
PE EXP SW TXN12	PEC16	0.22u4/X5R/6.3V/K	PE EXP SW TXN12_C
PE EXP SW TXP13	PEC17	0.22u4/X5R/6.3V/K	PE EXP SW TXP13_C
PE EXP SW TXN13	PEC18	0.22u4/X5R/6.3V/K	PE EXP SW TXN13_C
PE EXP SW TXP14	PEC19	0.22u4/X5R/6.3V/K	PE EXP SW TXP14_C
PE EXP SW TXN14	PEC20	0.22u4/X5R/6.3V/K	PE EXP SW TXN14_C
PE EXP SW TXP15	PEC21	0.22u4/X5R/6.3V/K	PE EXP SW TXP15_C
PE EXP SW TXN15	PEC22	0.22u4/X5R/6.3V/K	PE EXP SW TXN15_C

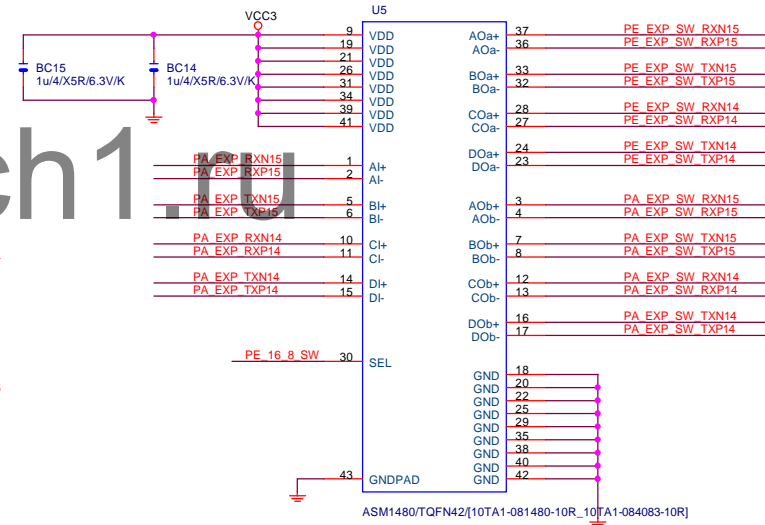


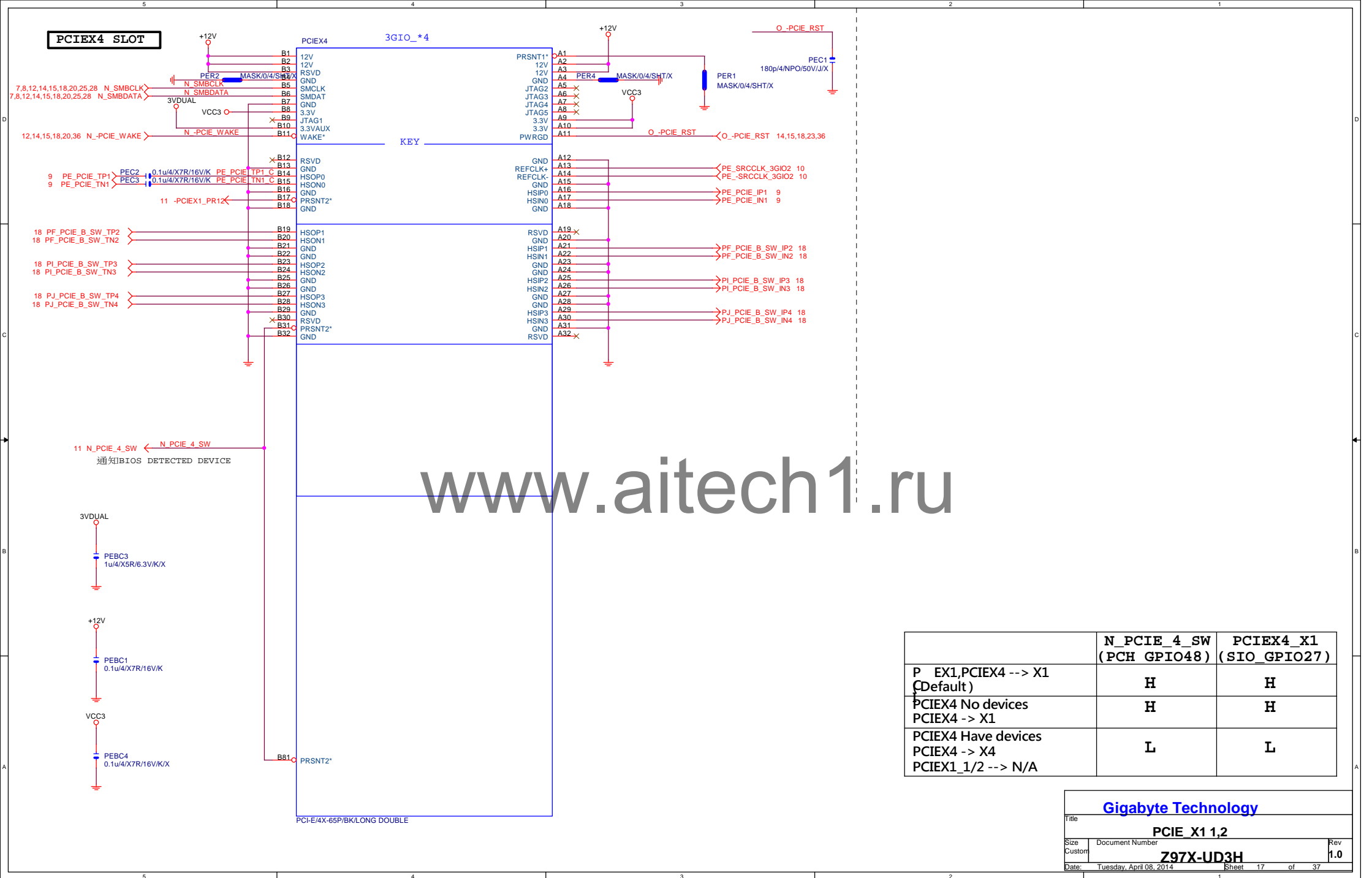
Function	SEL
xI--> xOa	L
xI--> xOb	H



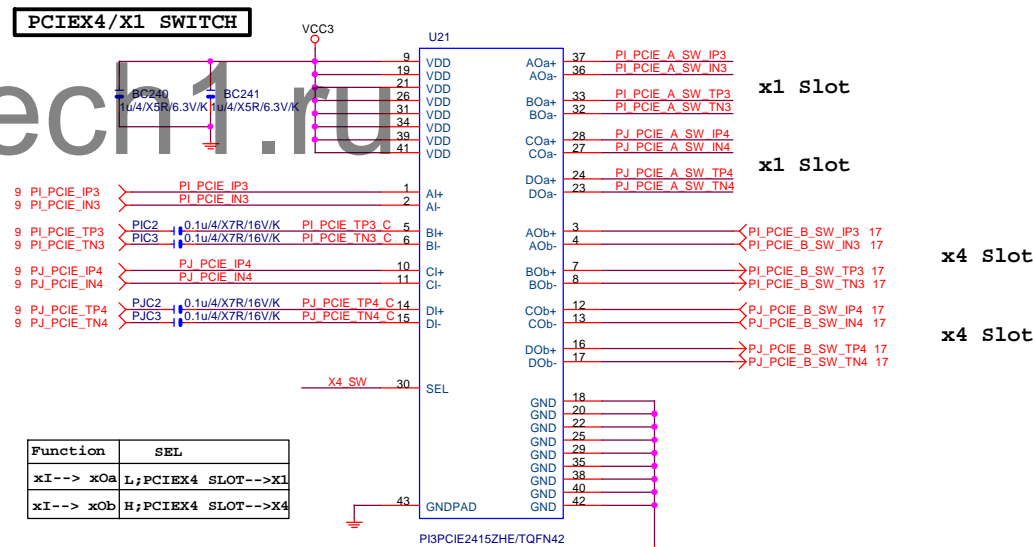
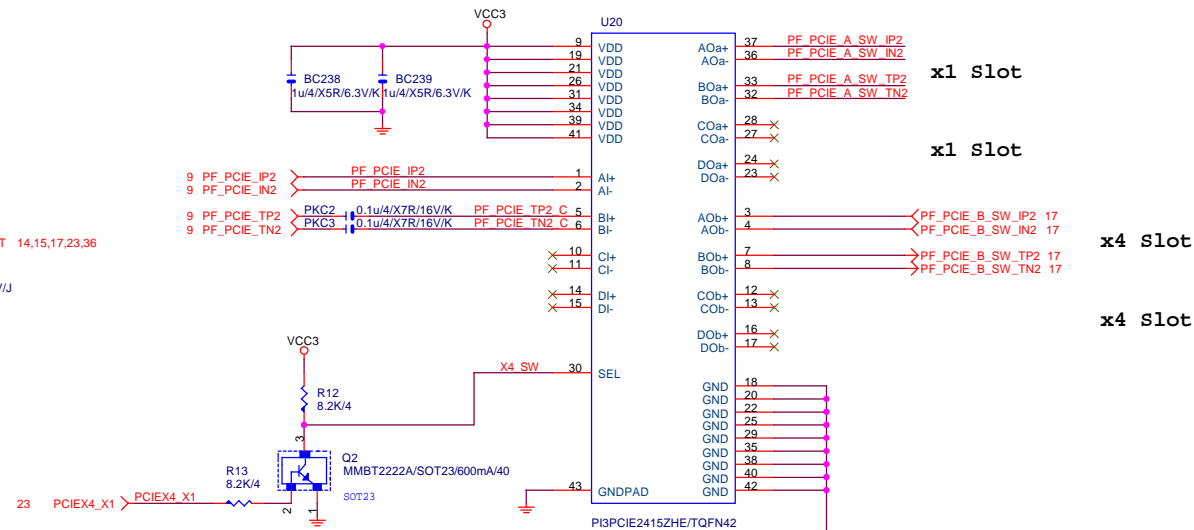
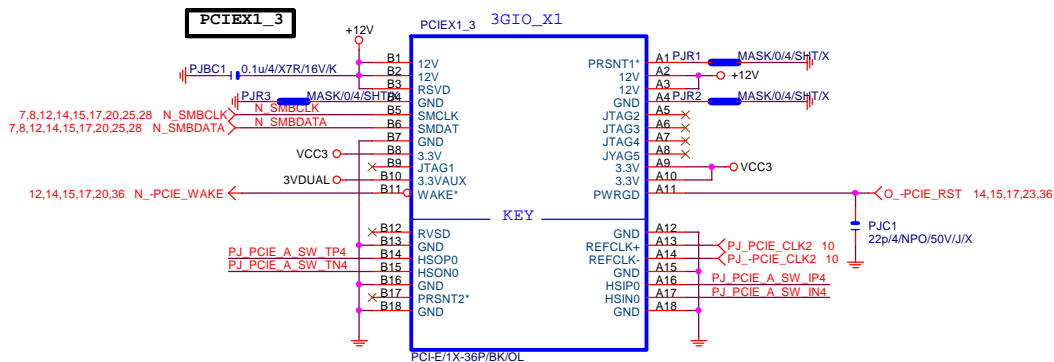
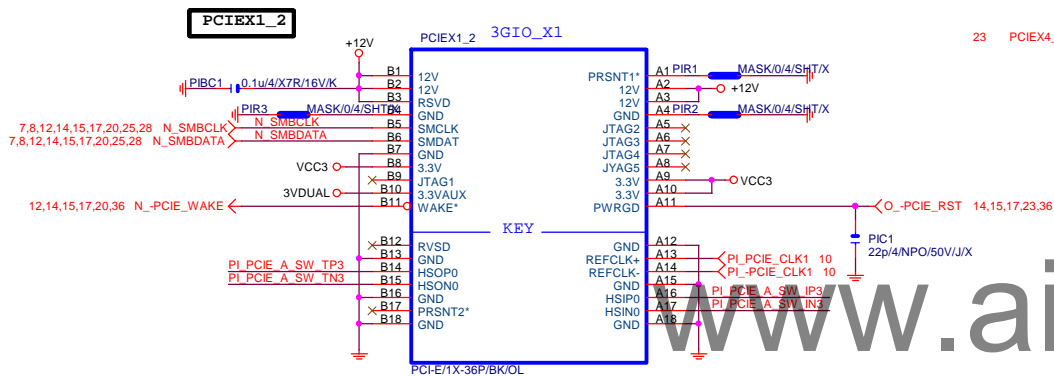
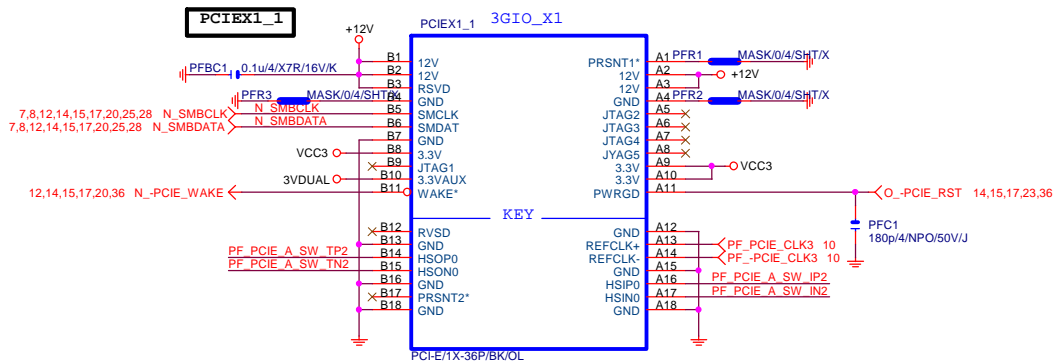
www.aitech1.ru

PA_EXP_SW_RXP[8..15] 14
PA_EXP_SW_RXN[8..15] 14
PA_EXP_SW_TXP[8..15] 14
PA_EXP_SW_TXN[8..15] 14
PE_EXP_SW_RXP[8..15] 15
PE_EXP_SW_RXN[8..15] 15
PE_EXP_SW_TXP[8..15] 15
PE_EXP_SW_TXN[8..15] 15
PA_EXP_RXP[0..15] 4,14
PA_EXP_RXN[0..15] 4,14
PA_EXP_TXP[0..15] 4,14
PA_EXP_TXN[0..15] 4,14

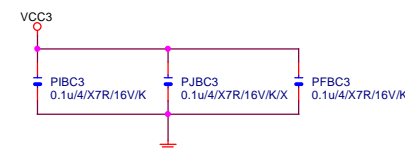


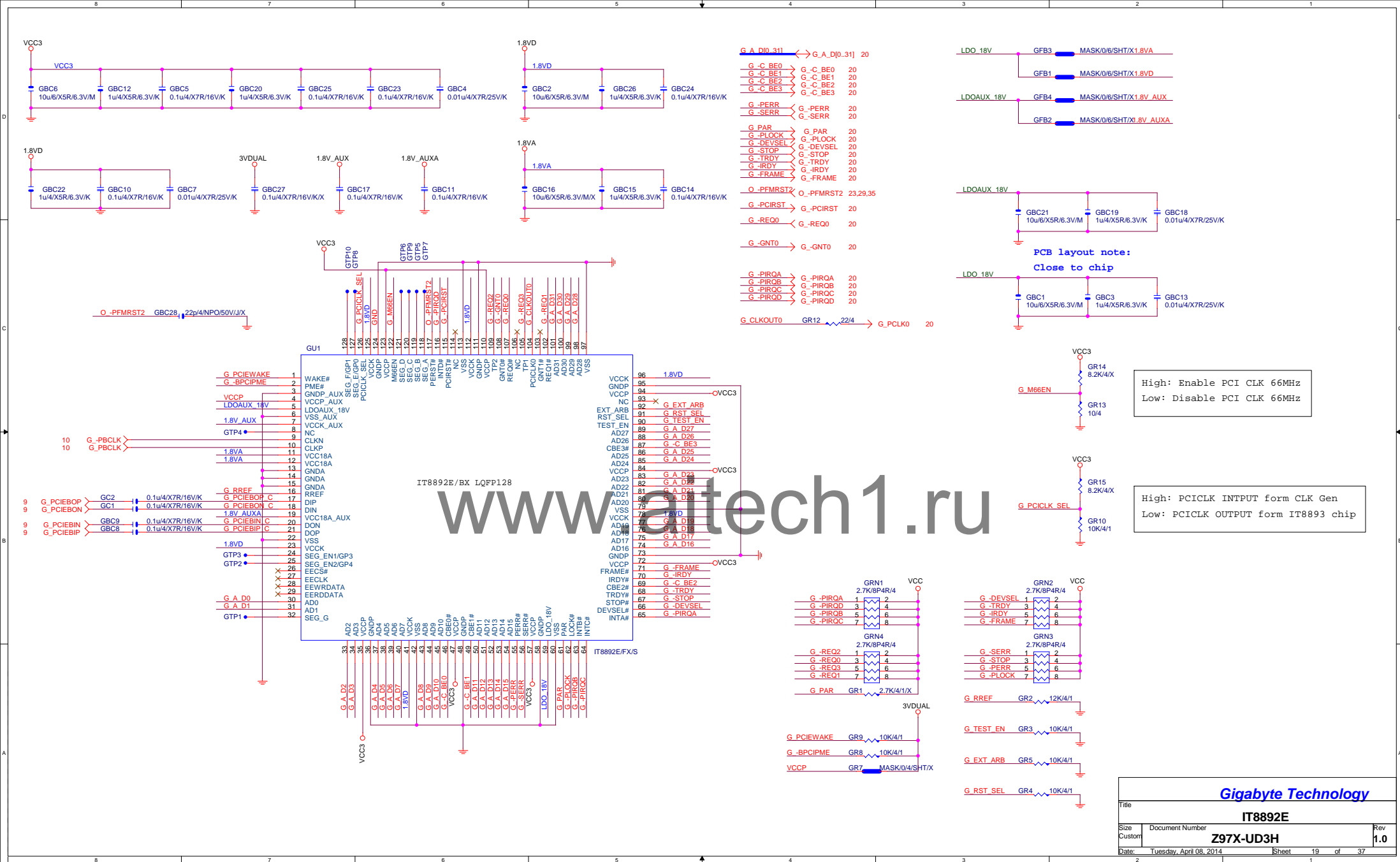


PCIEX1 SLOT



Function	SEL
xI--> xOa	L;PCIEX4 SLOT-->
xI--> xOb	H;PCIEX4 SLOT-->





AZALIA CODEC

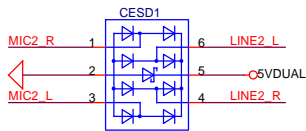
Thermal pad is DGND

Thermal pad is DGND

Digital Area

Analog Area

0/6/X For AGND/GND
moat under Codec
_Body



MASK/AZC099-04S.R7G/SOT23-6L[10DEF-550099-20R_10TA1-018902-10R]/X

EAPD: Default L
H : ON
L : OFF

Close to ALC1150

- BOM OPTION : 1. 台固/日固/日黑固/MUSE MW音效電容
2. 金屬外罩 Reserve
3. LED Reserve (若LED有上,G_PLED p-up請上CR130)

有LED機種,請上CR130

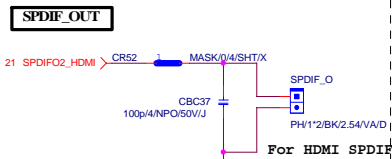
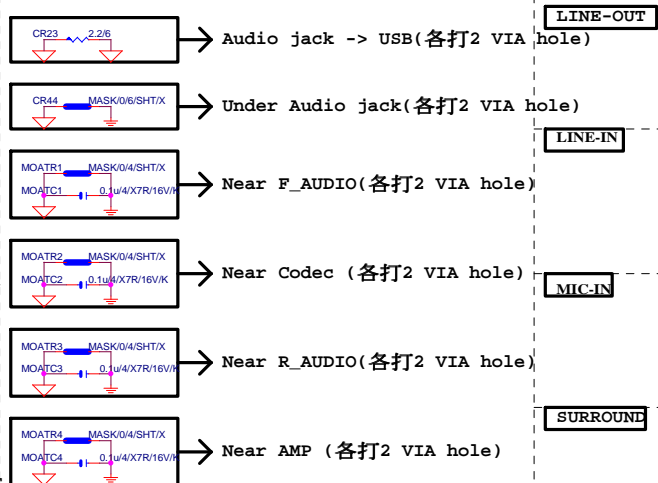
G_PLED
(IT8620 GP26)

MOAT LED

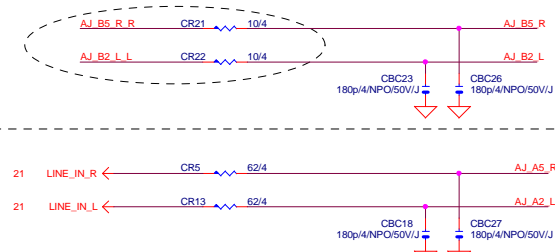
MASK/2N7002/SOT23/25pF/5/X
MASK/2N7002/SOT23/25pF/5/X

Gigabyte Technology

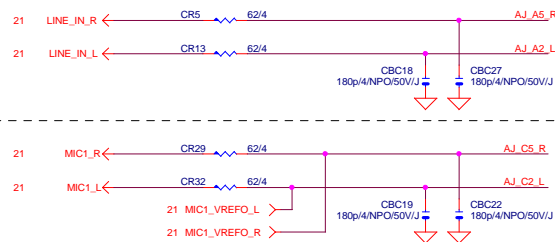
Title			HD AUDIO ALC887B-VD2/VT1708S/VT2021
Size	Document Number	Z97X-UD3H	
Custom		Rev 1.0	
Date:	Tuesday, April 08, 2014	Sheet	21 of 37



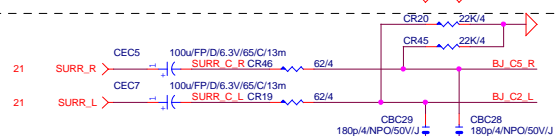
LINE-OUT



LINE-IN

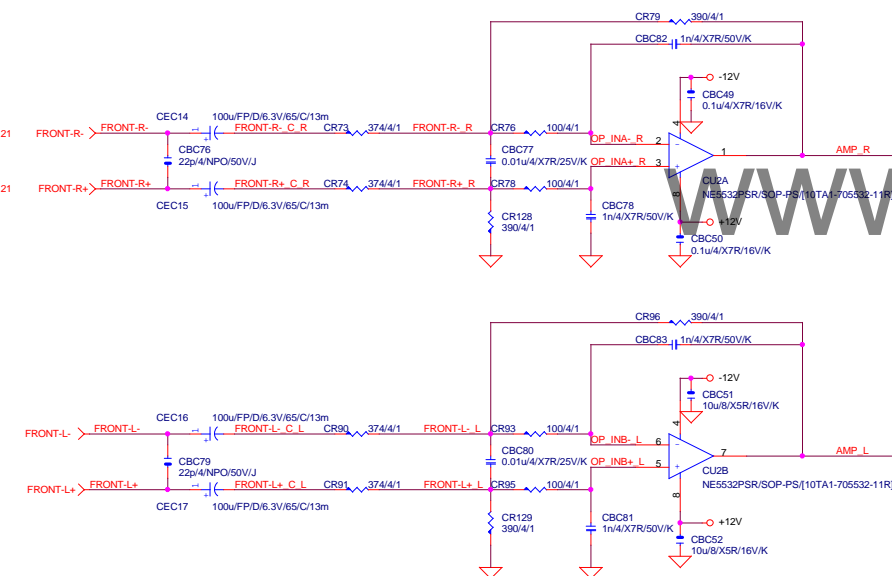


MIC-IN

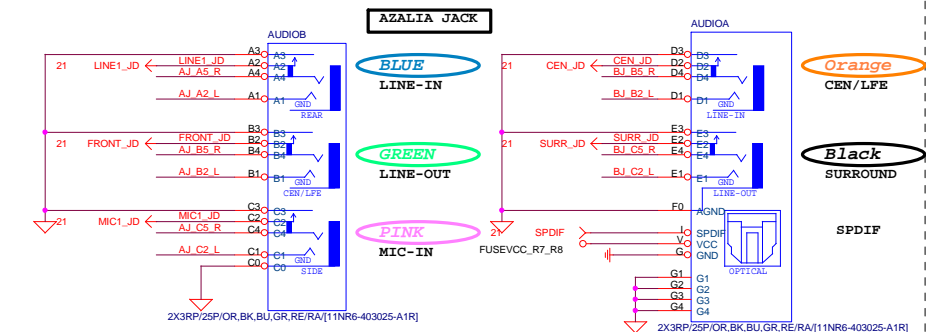
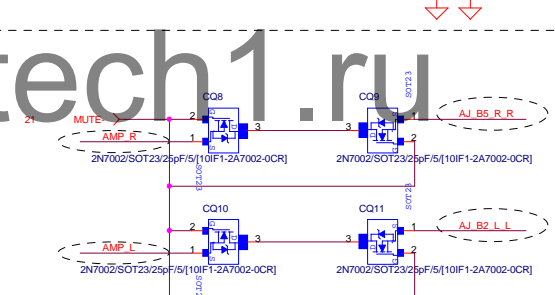
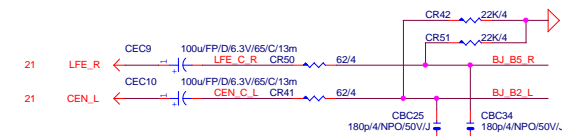


SURROUND

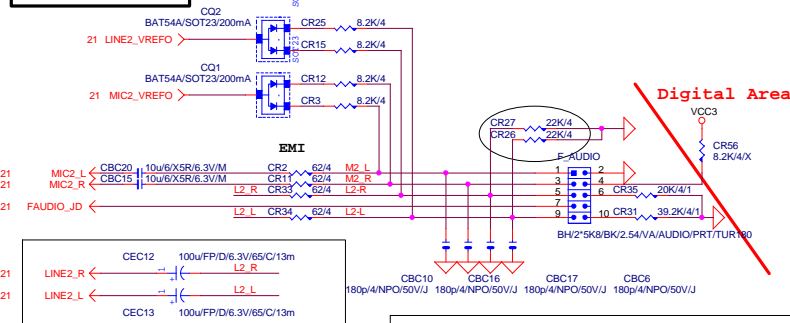
Differential to Single-End AMPLIFIED



CEN/LFE



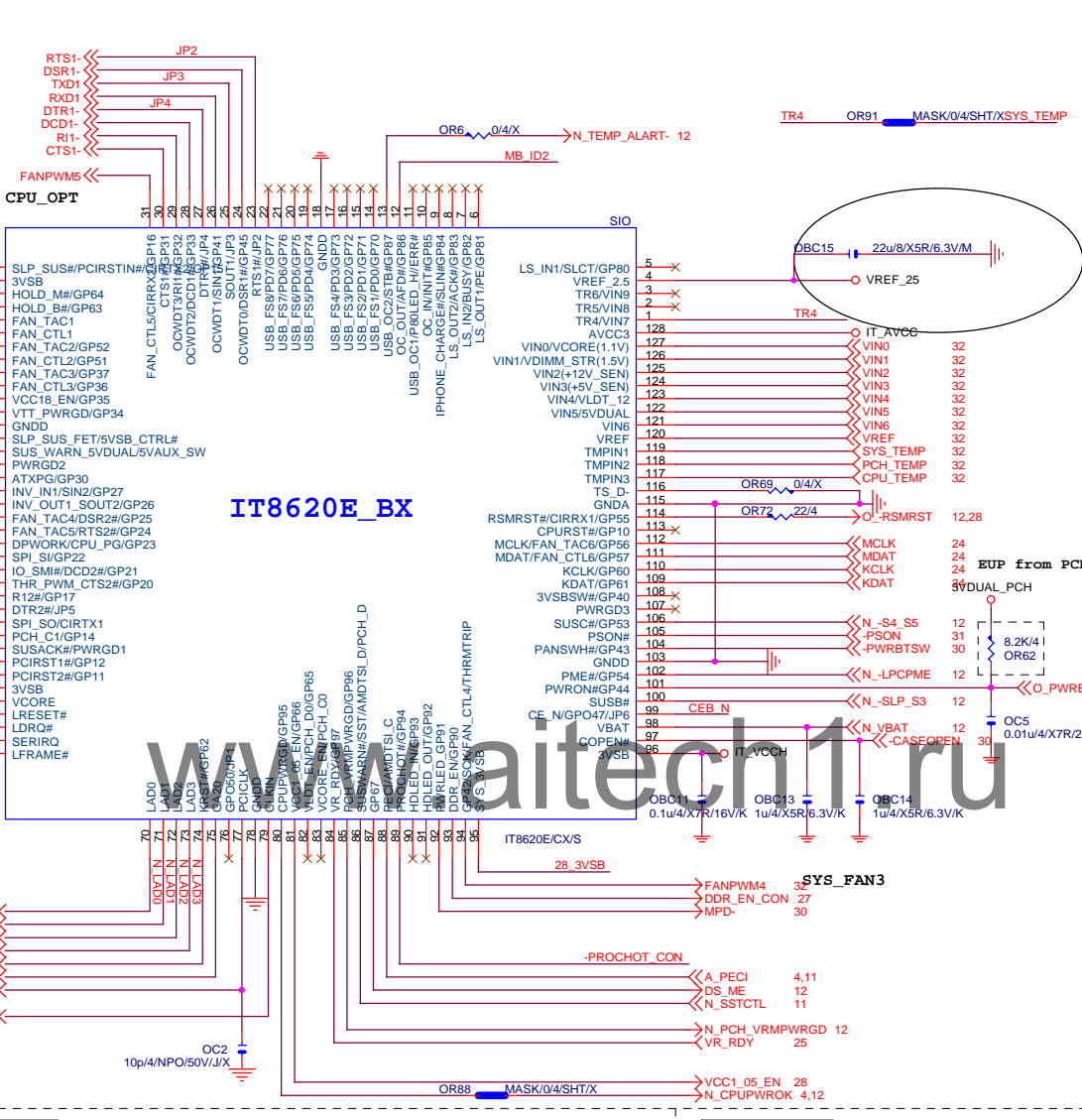
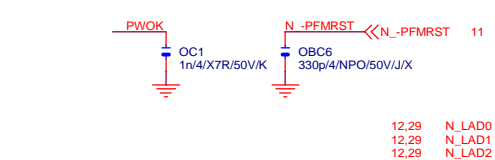
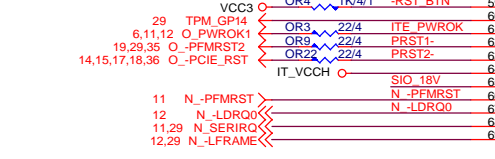
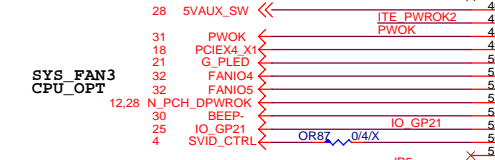
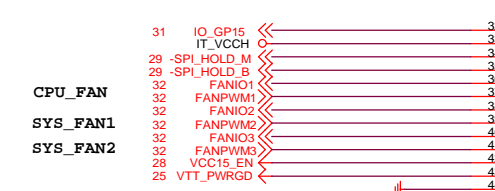
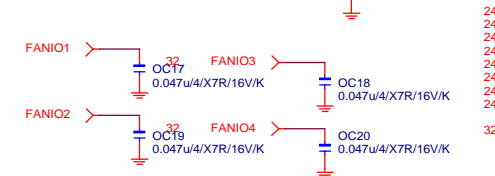
AZALIA FRONT PANEL



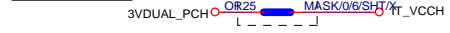
Gigabyte Technology

Title			
AUDIO JACK			
Size Custom	Document Number	Z97X-UD3H	Rev 1.0
Date:	Tuesday, April 08, 2014	Sheet 22 of 37	

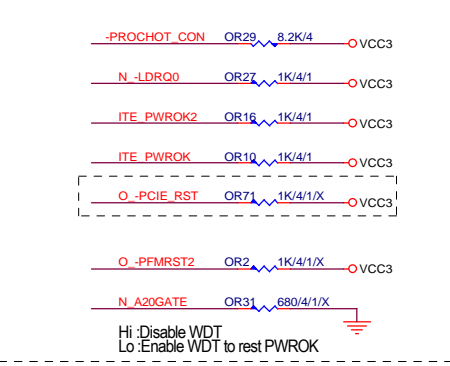
SIO IT8728F



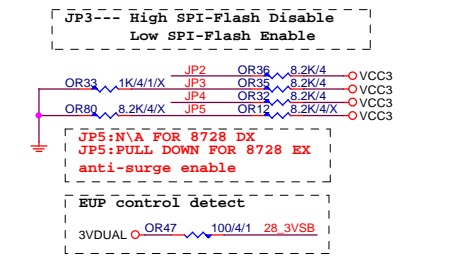
PWR SHT



SIO PU



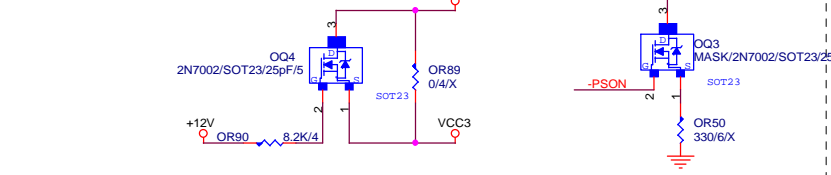
SIO STRAP



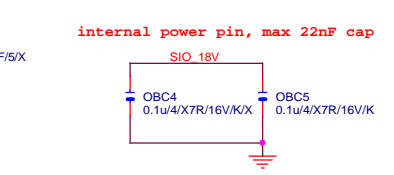
JP4	1	k8 power sequency function is Disable
	0	k8 power sequency function is Enable
JP3	1 1	The default value of EC Index 63h/6Bh/73h is 80h.
	1 0	The default value of EC Index 63h/6Bh/73h is FFh.
JP5	0 1	The default value of EC Index 63h/6Bh/73h is 00h.
	0 0	The default value of EC Index 63h/6Bh/73h is 40h.

IT8620E GPIO問題匯整	
PIN 50	GP26--- 第一次接上POWER時會拉 LO
PIN 90/91	DEFAULT為HLED FUNCTION, GP93 BYPASS TO GP92 高溫時 GP92 會被拉LO(ITE BUG)
PIN 108	GP40--- POWER ON 時會拉 LO
PIN 111/112	MOUSE 跟FAN6 FUNCTION 擇一使用, 不然會互相干擾

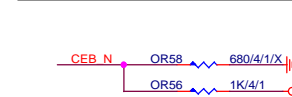
Power leakage



SIO 18V



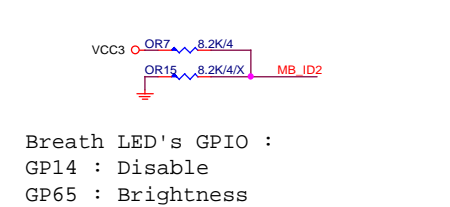
DUAL BIOS OPT STRAP



SIO CAP



MB ID



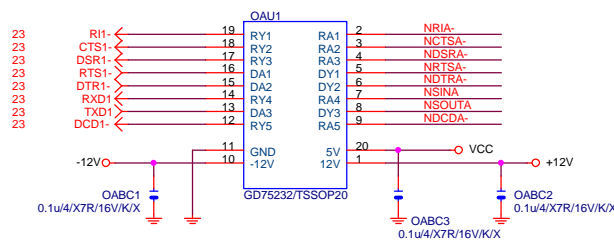
Gigabyte Technology

Title: ITE 8620CX LPC IO

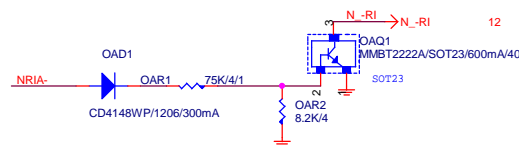
Size B Document Number: Z97X-UD3H Rev 1.0

Date: Tuesday, April 08, 2014 Sheet 23 of 37

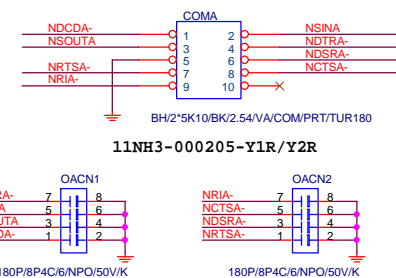
COMA



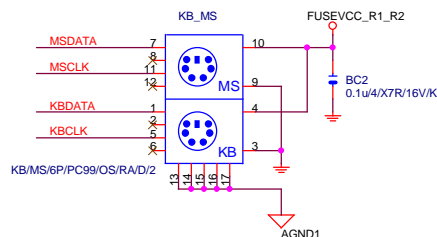
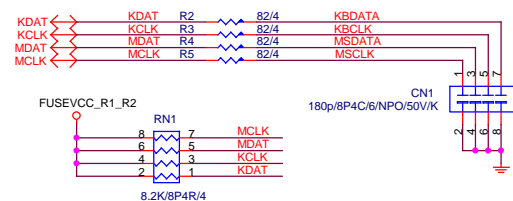
COM RI



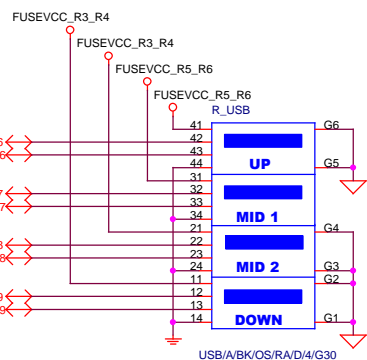
COM BUFFER



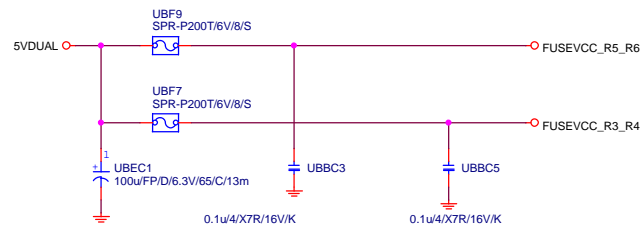
KB/USB



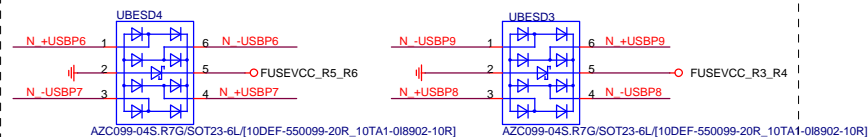
R_USB



USB20 FUSE



USB20 ESD PROTECT

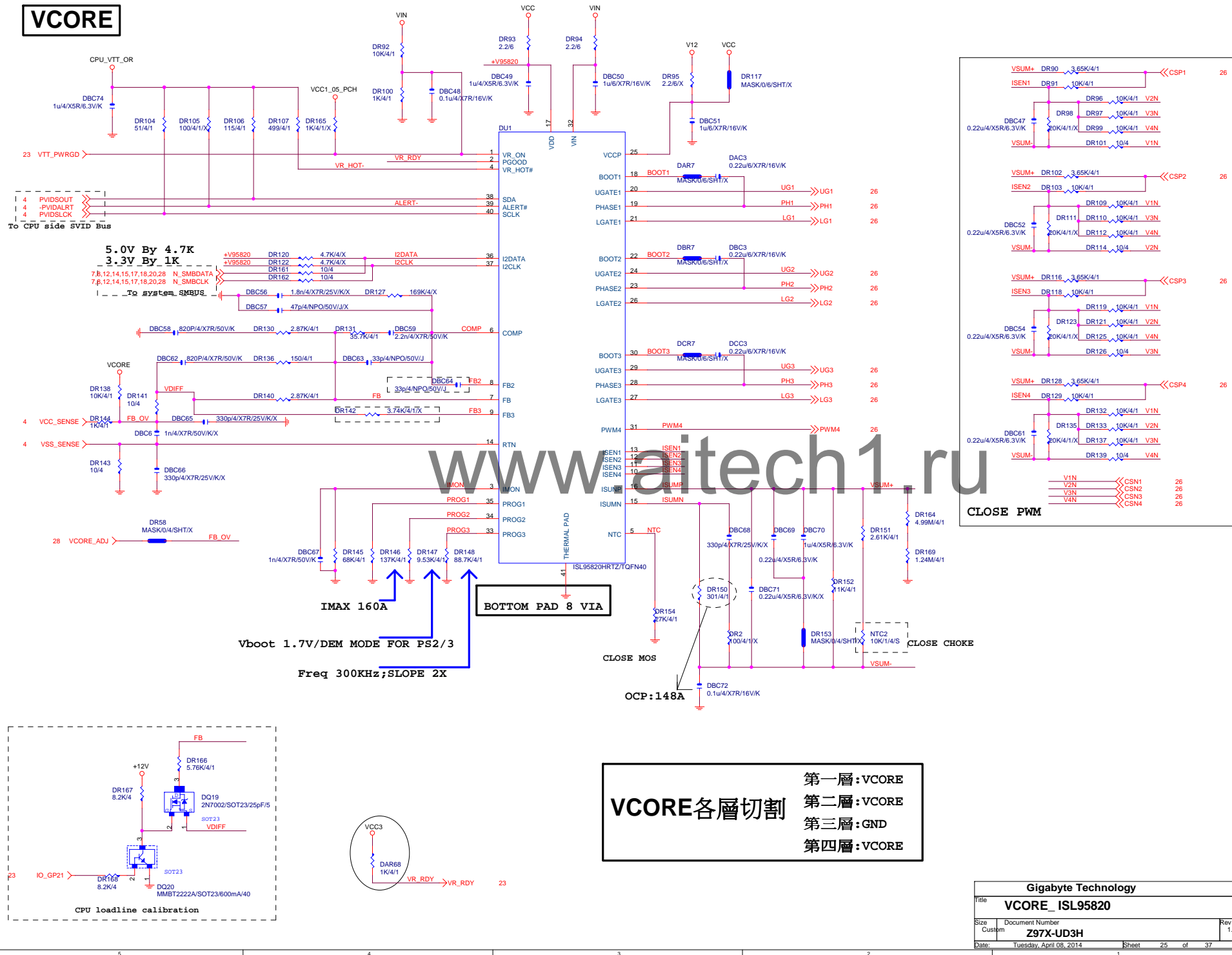


www.aitech1.ru

Gigabyte Technology

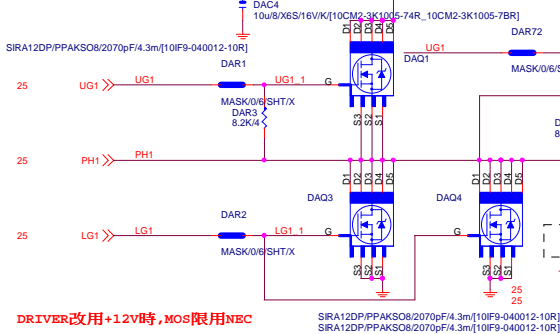
Title			
COM/ PROHOT/ R_USB			
Size	Document Number	Rev	
Custom		Z97X-UD3H	
Date:	Tuesday, April 08, 2014	Sheet	24 of 37

VCORE



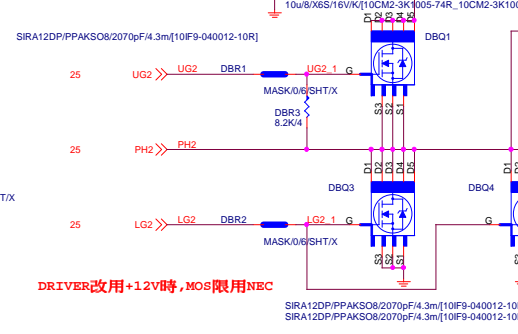
VCORE

[1]



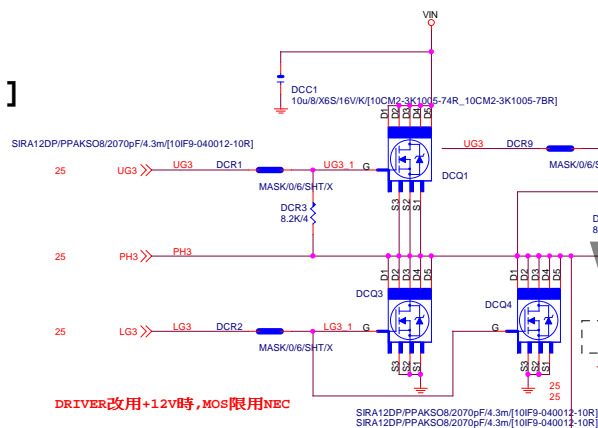
DRIVER改用+12V時,MOS限用NEC

[2]



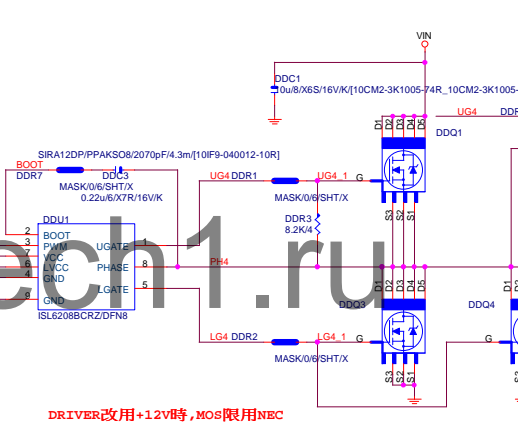
DRIVER改用+12V時,MOS限用NEC

[3]



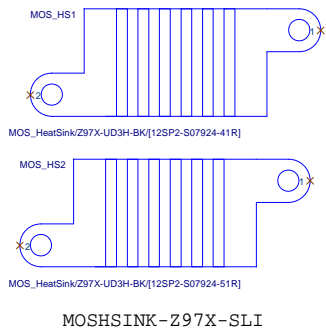
DRIVER改用+12V時,MOS限用NEC

[4]



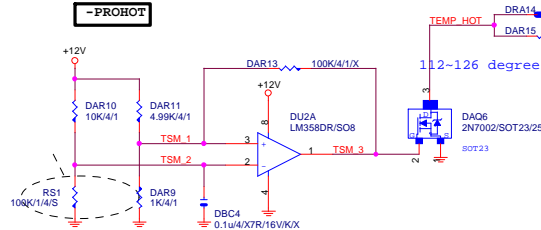
DRIVER改用+12V時,MOS限用NEC

MOSFET HEATSINK

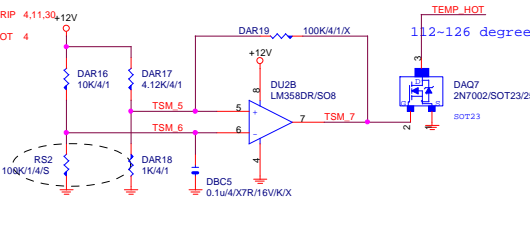


MOSHHSINK-Z97X-SLI

-PROHOT



TEMP HOT 112-126 degree

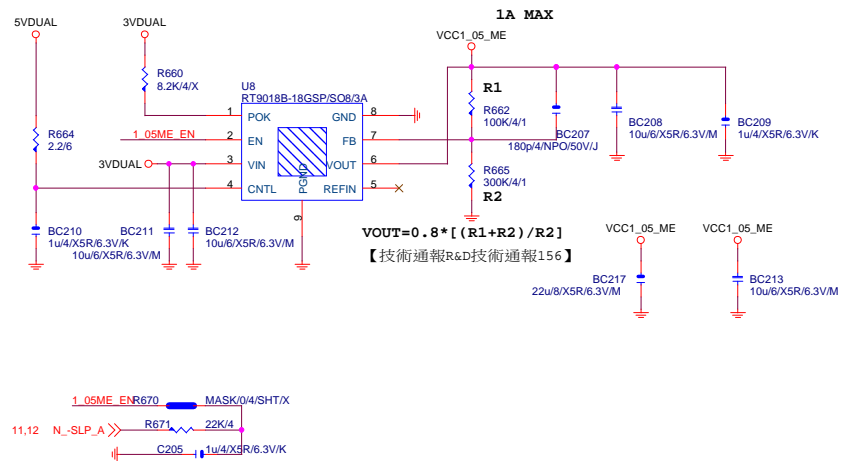


TEMP HOT 112-126 degree

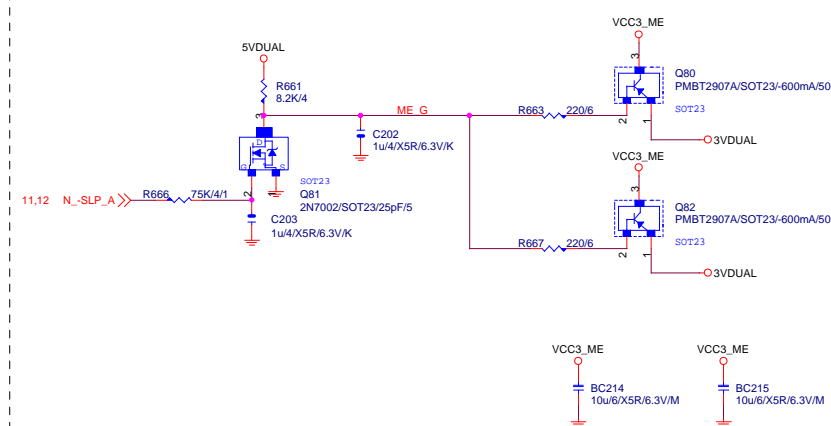
Gigabyte Technology

Title	ISL95820_2
Size	Document Number
Custom	Z97X-UD3H
Date	Tuesday, April 08, 2014
Sheet	26 of 37
Rev	1.0

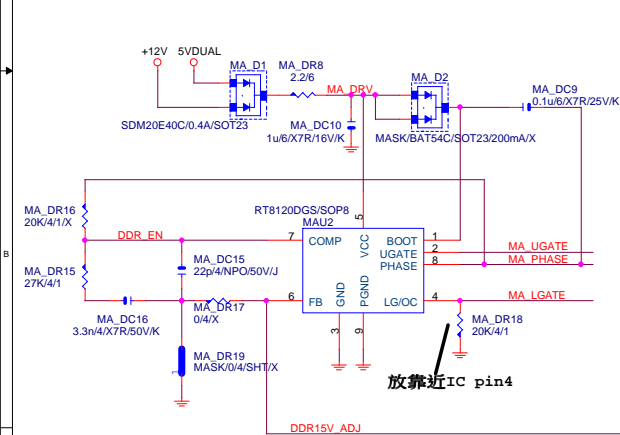
VCC1_05_ME



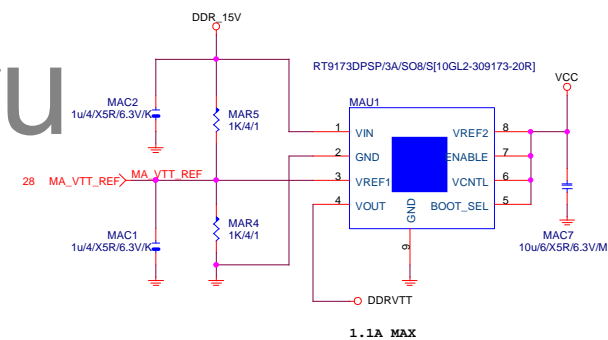
VCC3_ME



DDR 15V



DDRVTT



VIN=5V, VOUT=1.5V, IOUT=25A, PHASE=1
IRMS=11.45A

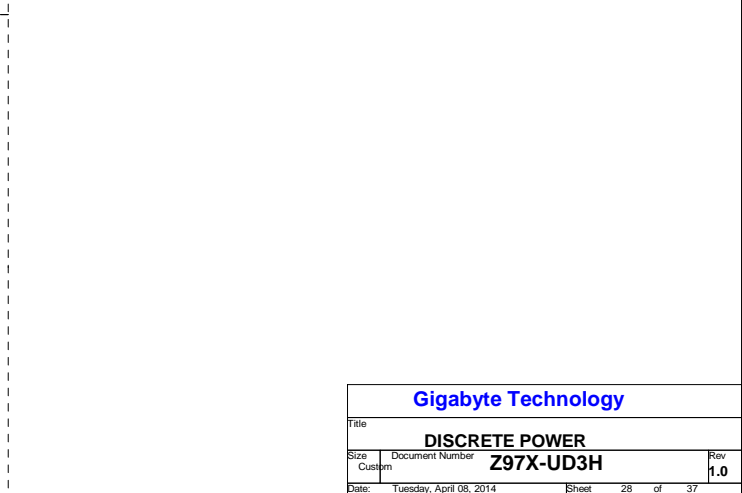
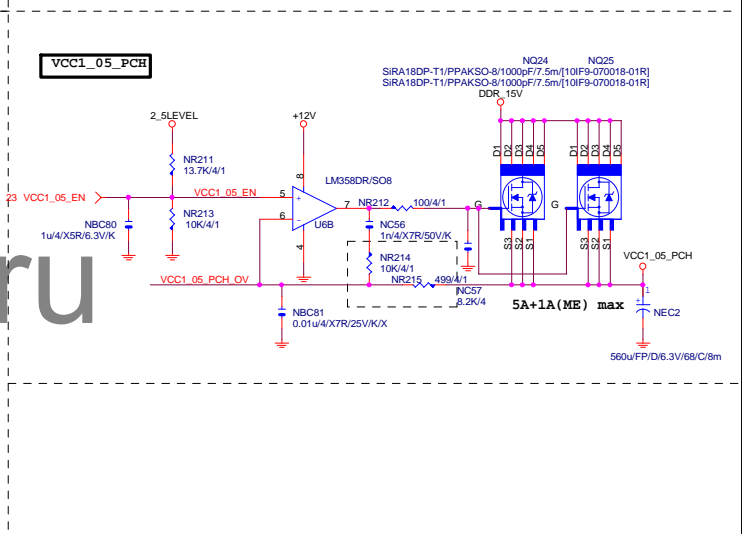
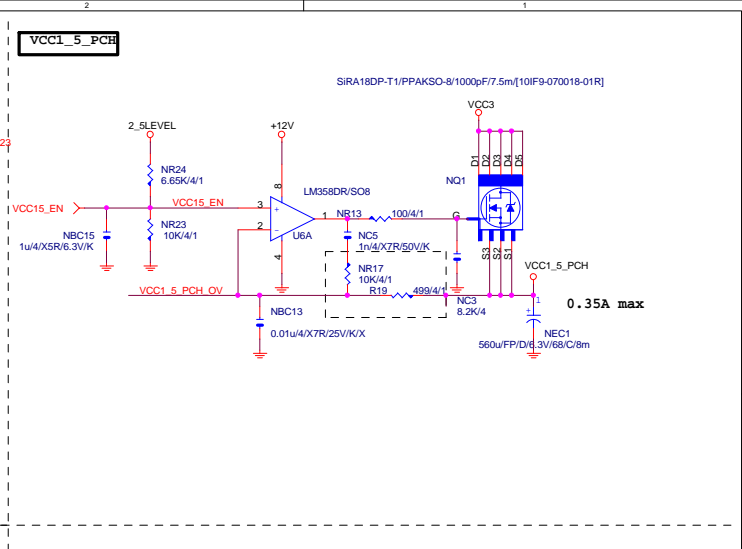
560u/FP/D/6.3V/68/8m RIPPLE CURRENT=4.7A
Coefficient=1.7(85°C), 1(105°C)

VIN Ripple current=4.7X1.7=7.99A(85°C)
-->故固態電容須2X7.99=15.98>11.45A

OCP:35.82A for Rds=6.7m for vishay@4.5V
OCP:72.727A for Rds=3.3m for renesas@10V
OCP:48A=RoSet*Iocset / Rds(on)
=12K*10uA / [5/5]

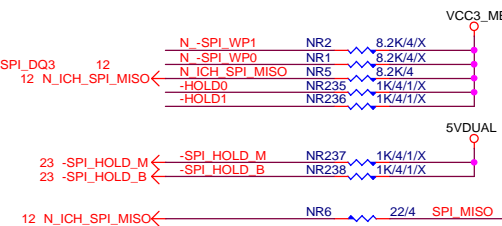
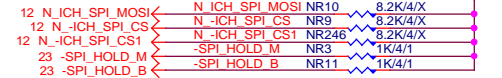
GIGABYTE™

Title		
DDR15V / M3 POWER		
Size	Document Number	Rev
Custom	Z97X-UD3H	1.0
Date:	Tuesday, April 08, 2014	Sheet 27 of 37



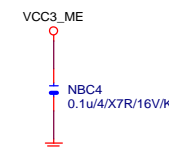
DUAL BIOS

MOSI For DMI RX Termination Voltage

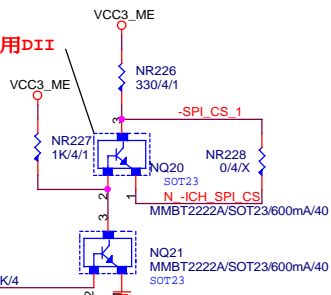


BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

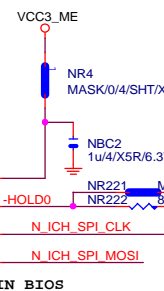
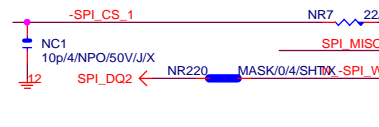
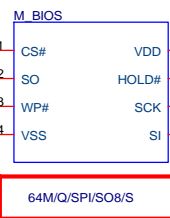
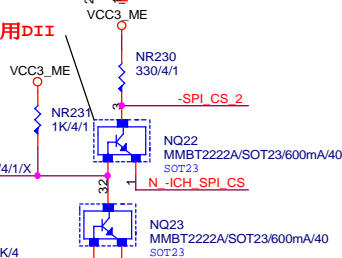
1 means floating
0 means PD 1K



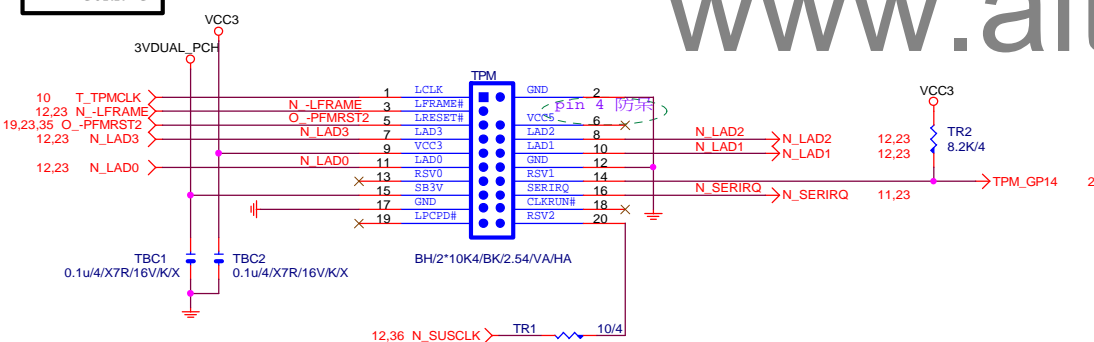
指定用DII



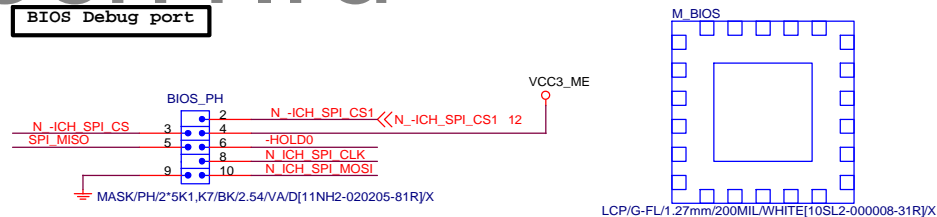
指定用DII



TPM CONNECT



BIOS Debug port

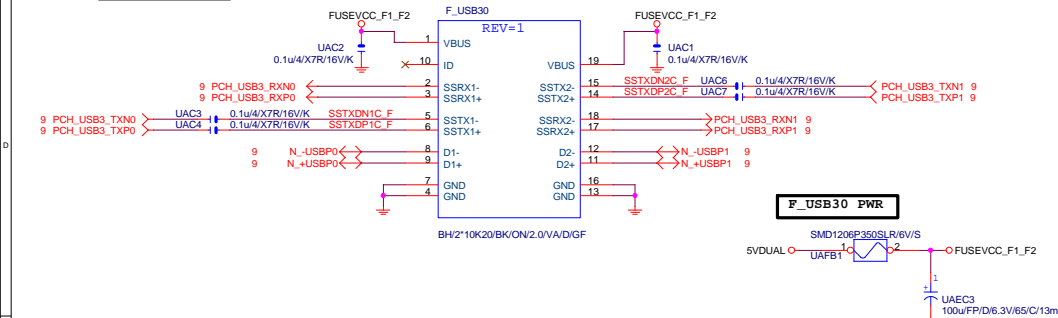


LCP/G-FL/1.27mm/200MIL/WHITE[10SL2-000008-31R]/X

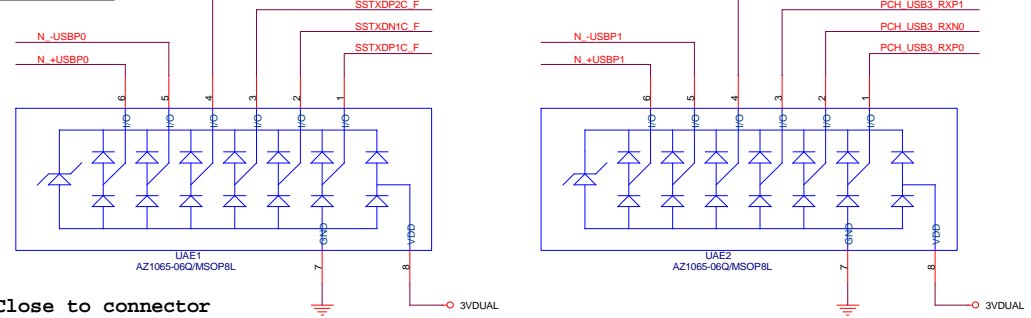
Gigabyte Technology

Title		BIOS	
Size	Document Number	Z97X-UD3H	
Custom		Rev	1.0
Date:	Tuesday, April 08, 2014	Sheet	29 of 37

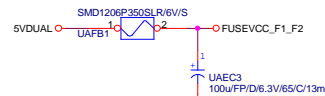
Front USB3.0



F_USB30 ESD PROTECT

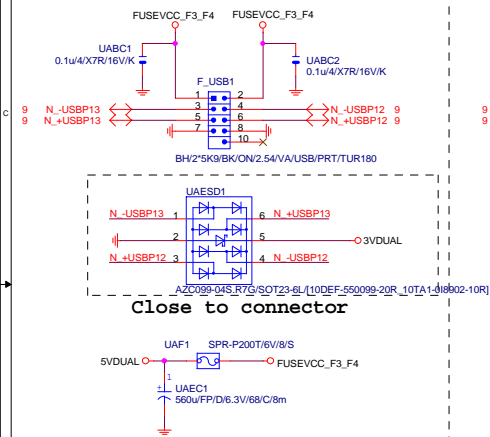


F_USB30 PWR

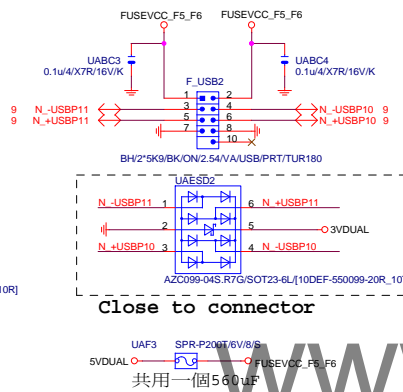


Close to connector

FRONT USB1

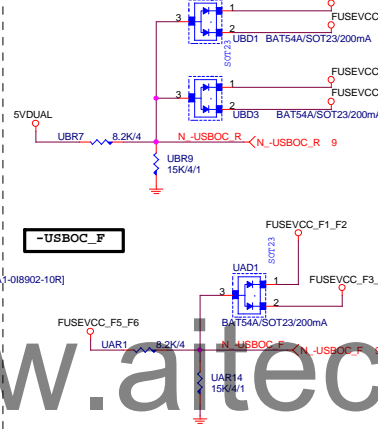


FRONT USB2

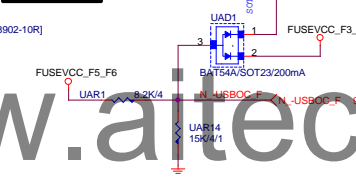


Close to connector

-USBOC_R

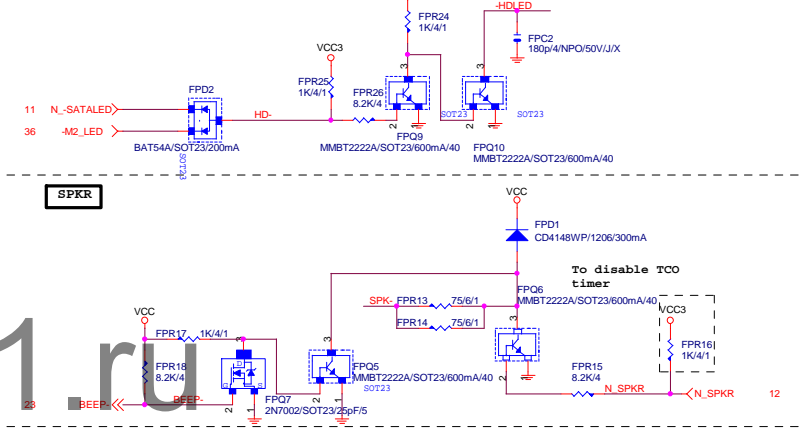


-USBOC_F

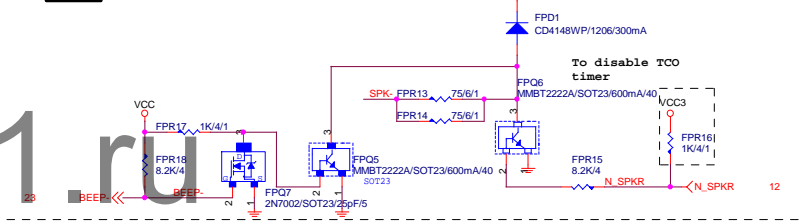


SATA LED

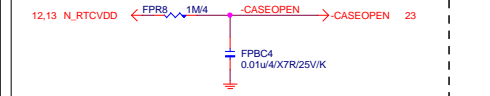
SATALED# signal open-collector, pull-up (8.2 kΩ to 10 kΩ) to Vcc3_3



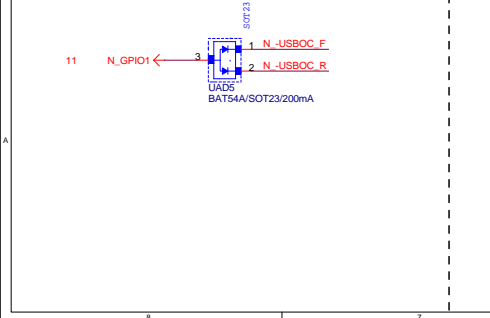
SPKR



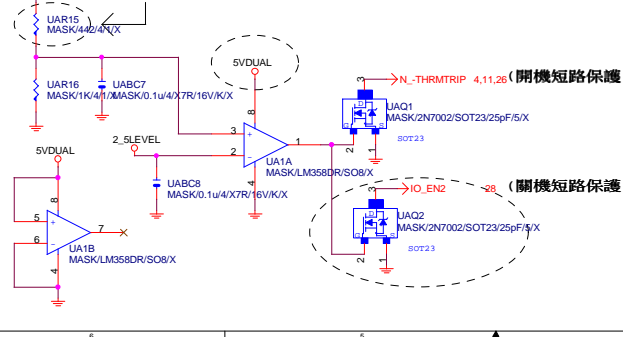
CASE OPEN



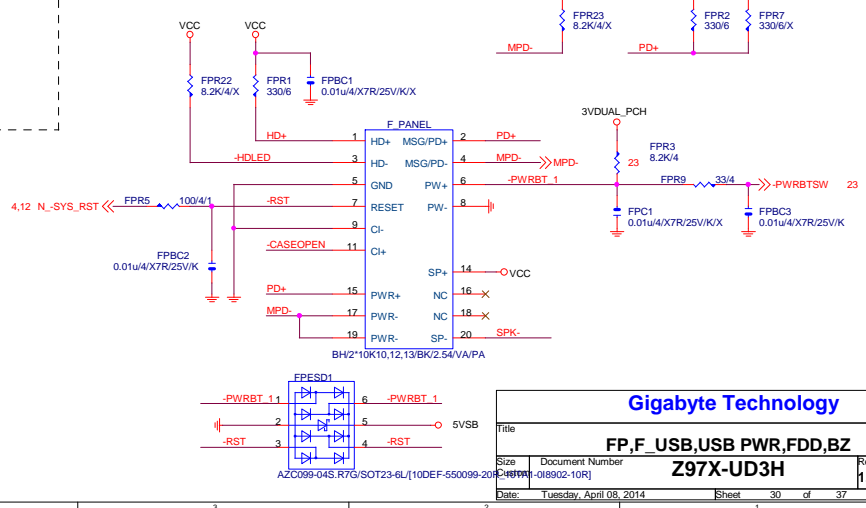
F_USB POWER PROTECT



USB2.0 Signal & power short protection
USB2.0 Signal > 4.85V
Enable --> 3VDUAL=3.6V

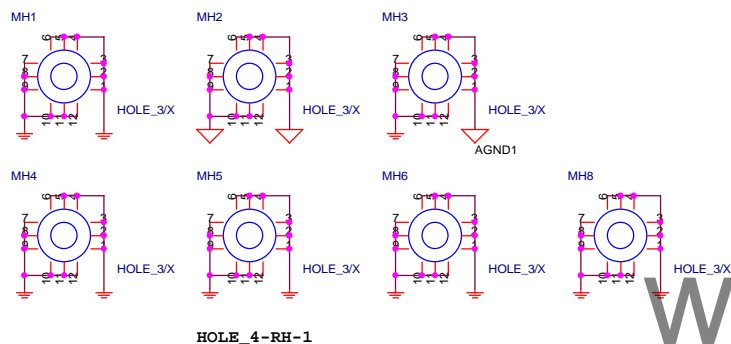
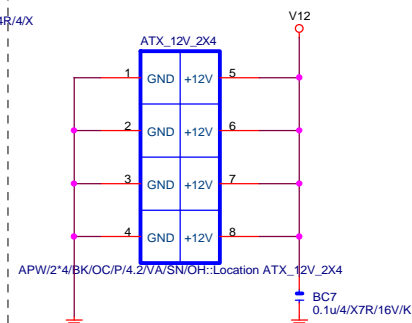
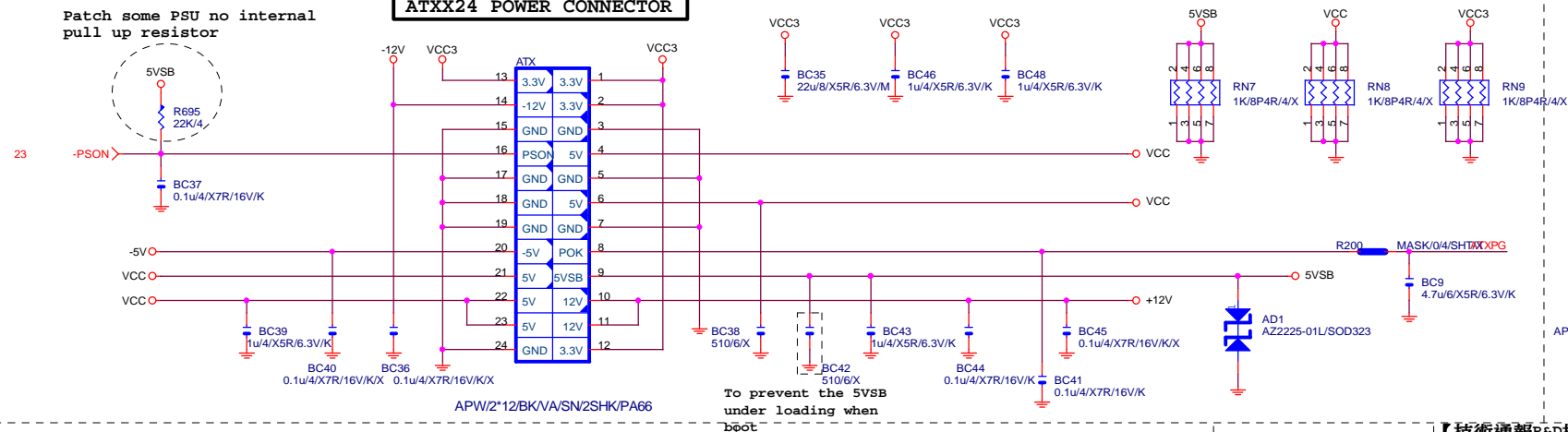


INTEL FRONT PANEL

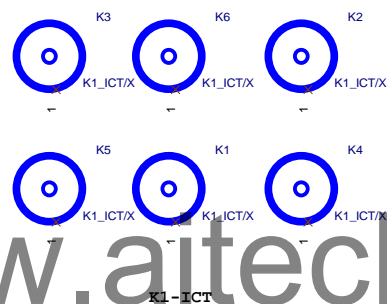


Gigabyte Technology

FP,F_USB,USB PWR,FDD,BZ		
Size	Document Number	Rev
4411	Z97X-UD3H	1.0
Date:	Tuesday, April 08, 2014	Sheet 30 of 37

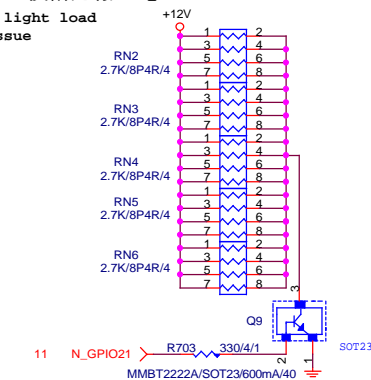


To prevent the 5VSB
under loading when
boot-----



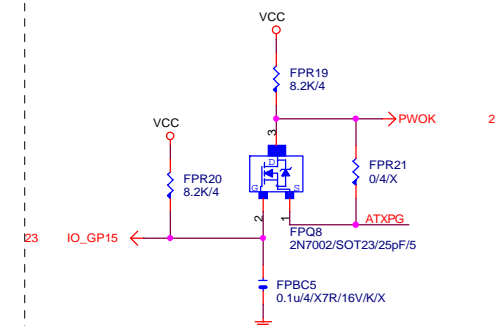
【技術通報R&D技術通報153】

To fix 12V light load
abnromal issue



PWOK PATCH

【技術通報R&D技術通報154】

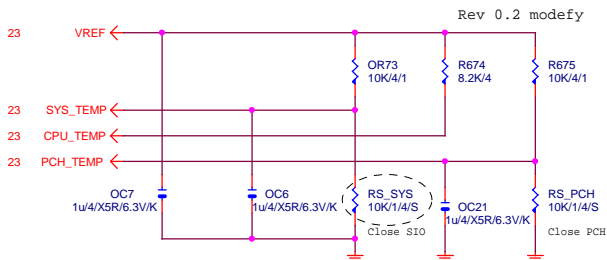


Gigabyte Technology

Title	ATX POWER CONNECTOR
-------	----------------------------

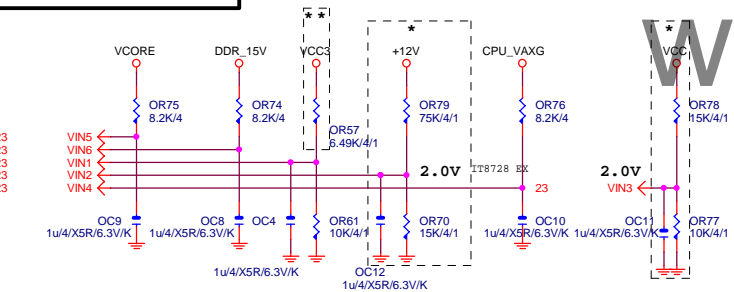
Size Custom	Document Number Z97X-UD3H	Rev 1.0
Date:	Tuesday, April 08, 2014	Sheet 31 of 37

TEMP H/W MONITOR



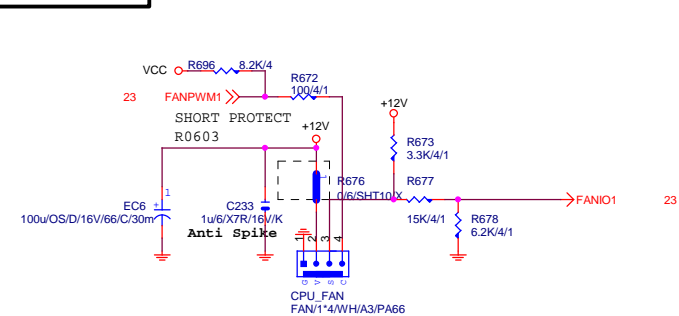
Thrmtrip#改用LM358做

VOLTAGE-- H/W MONITOR



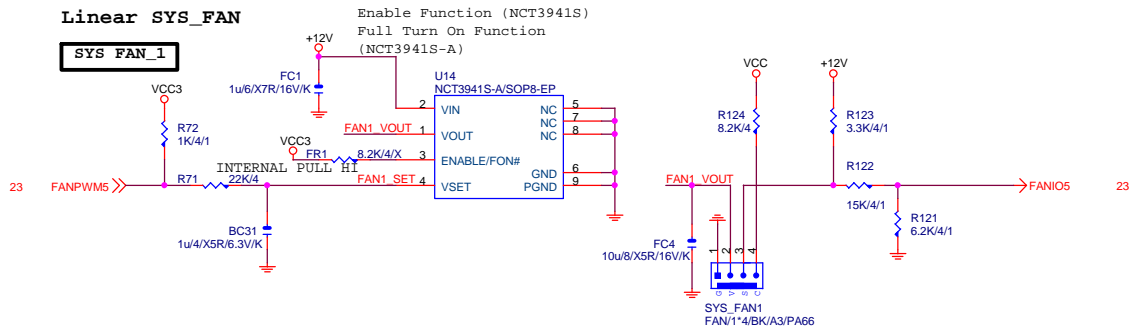
The division voltage of VIN2 & VIN3 must be around 2.9V

CPU SMART FAN

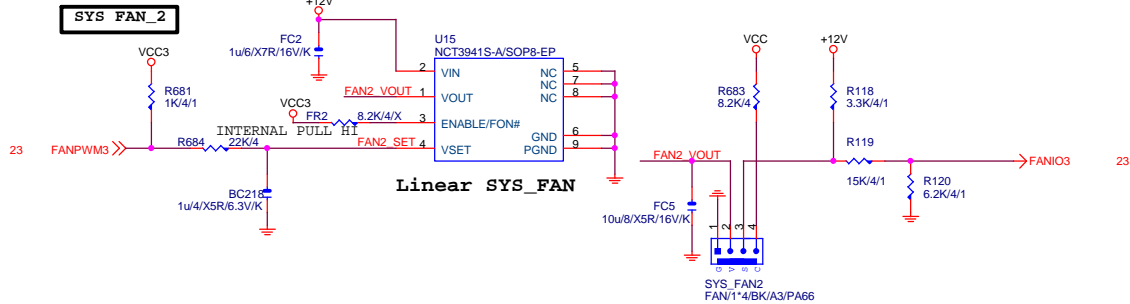


Linear SYS_FAN

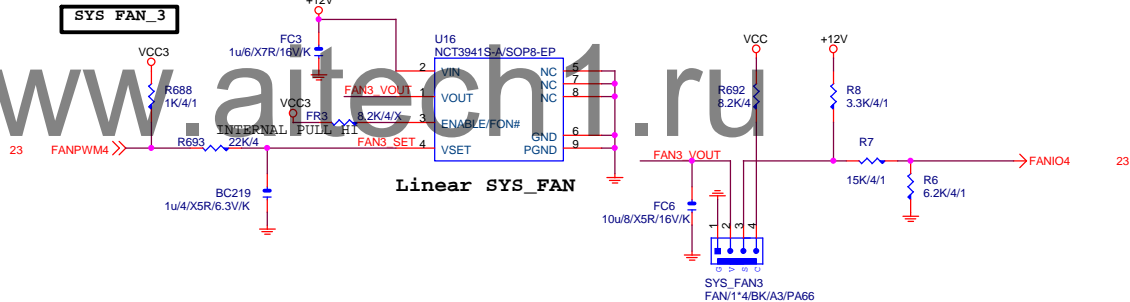
SYS FAN_1



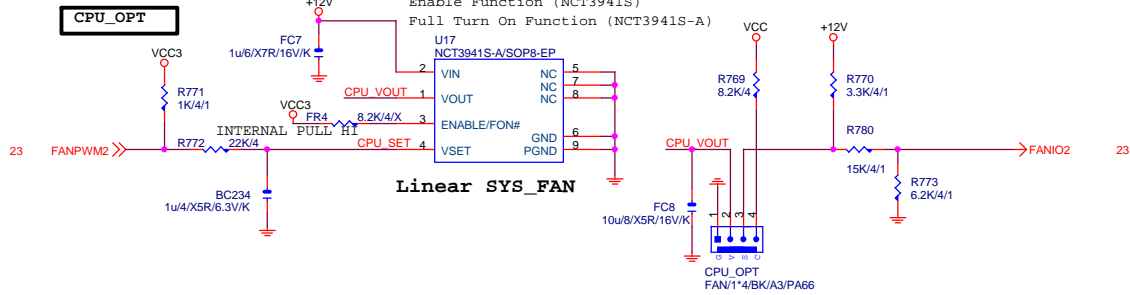
SYS FAN_2



SYS FAN_3



CPU_OPT



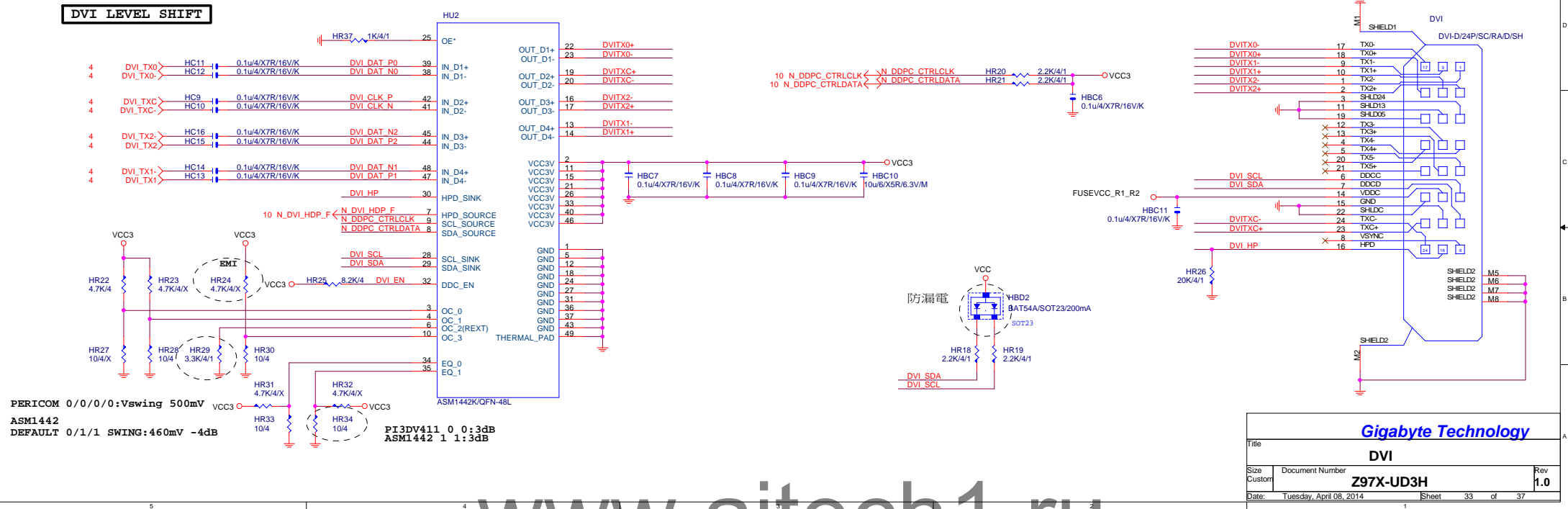
Gigabyte Technology

Title					HWM,KB/MS, FAN CTRL				
Size	Custom	Document Number				Rev			
		Z97X-UD3H				1.0			
Date:	Tuesday, April 08, 2014					Sheet	32	of	37

DVI LEVEL SHIFT

DVI:15/4/4/15

Impedance=85 +/- 17.5%

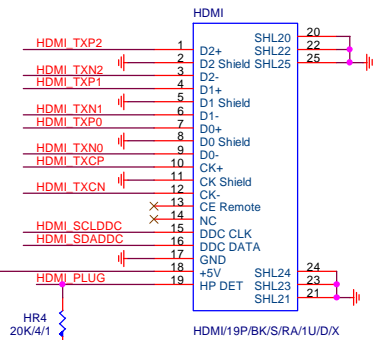
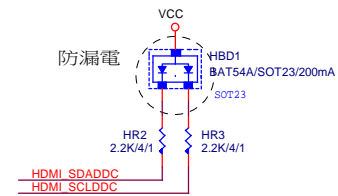
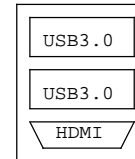
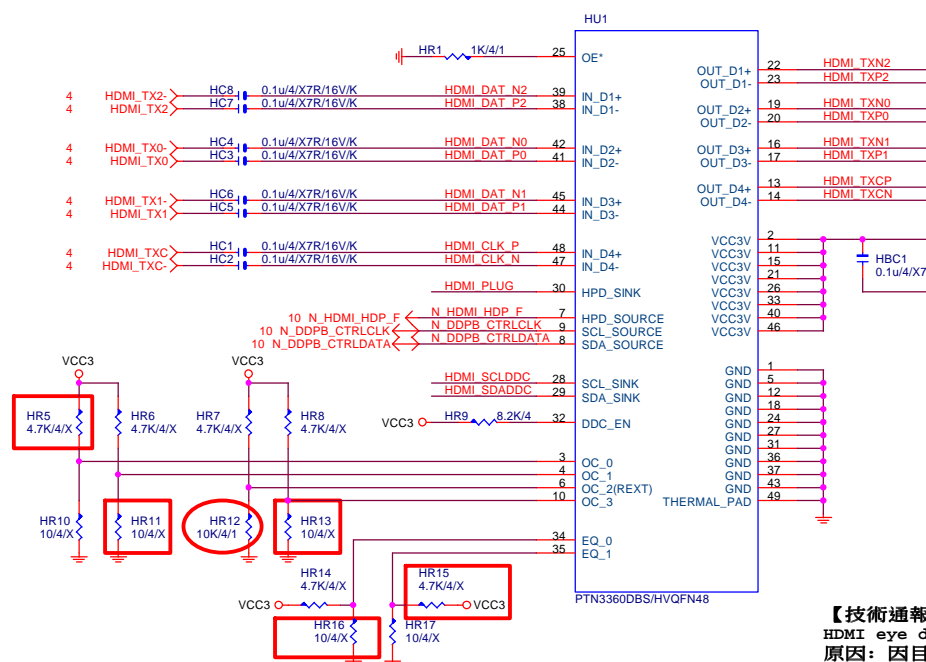


www.aitech1.ru

HDMI LEVEL SHIFT

HDMI: 20/4/6/4/20

Impedance=85 +- 17.5%



HDMI與R_USB共用一個料件

PTN3360:PIN 4/10/34/35 NC PIN,都不上值;只上HR12:10K
ASM1442:紅色框要上,HR12:3.16K

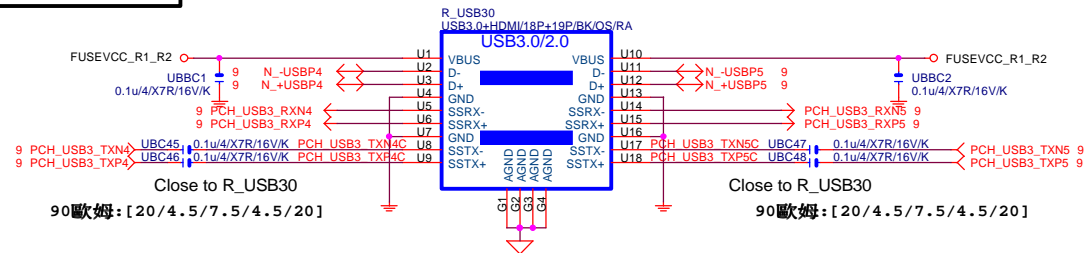
【技術通報R&D技術通報150】

HDMI eye diagram 1.4版(deep color)會fail

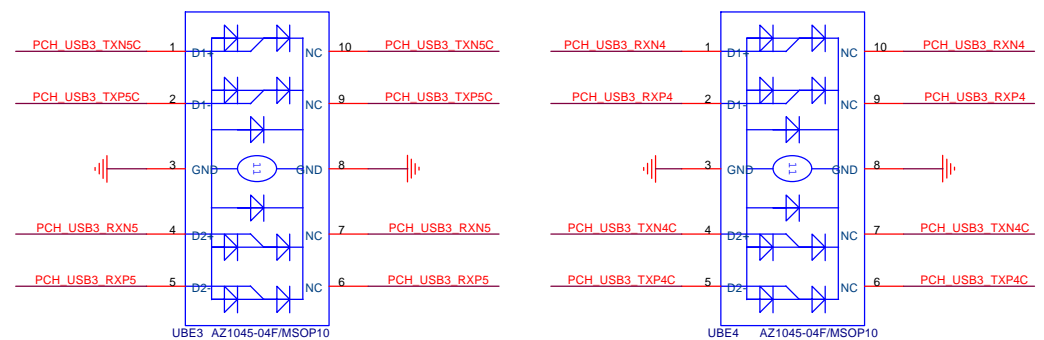
原因：因目前的HDMI訊號過長，造成RISING TIME過慢，而會壓到eye diagram

改善: ASMEDIA ASM1442 : 3.16K(PIN6 PULL DOWN電阻) 10ohm(PIN4 PULL DOWN電阻)

USB30_20 CONNECT

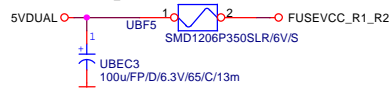


USB30 ESD PROTECT



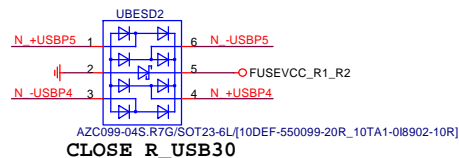
USB30 PWR

Polyswitch-1206



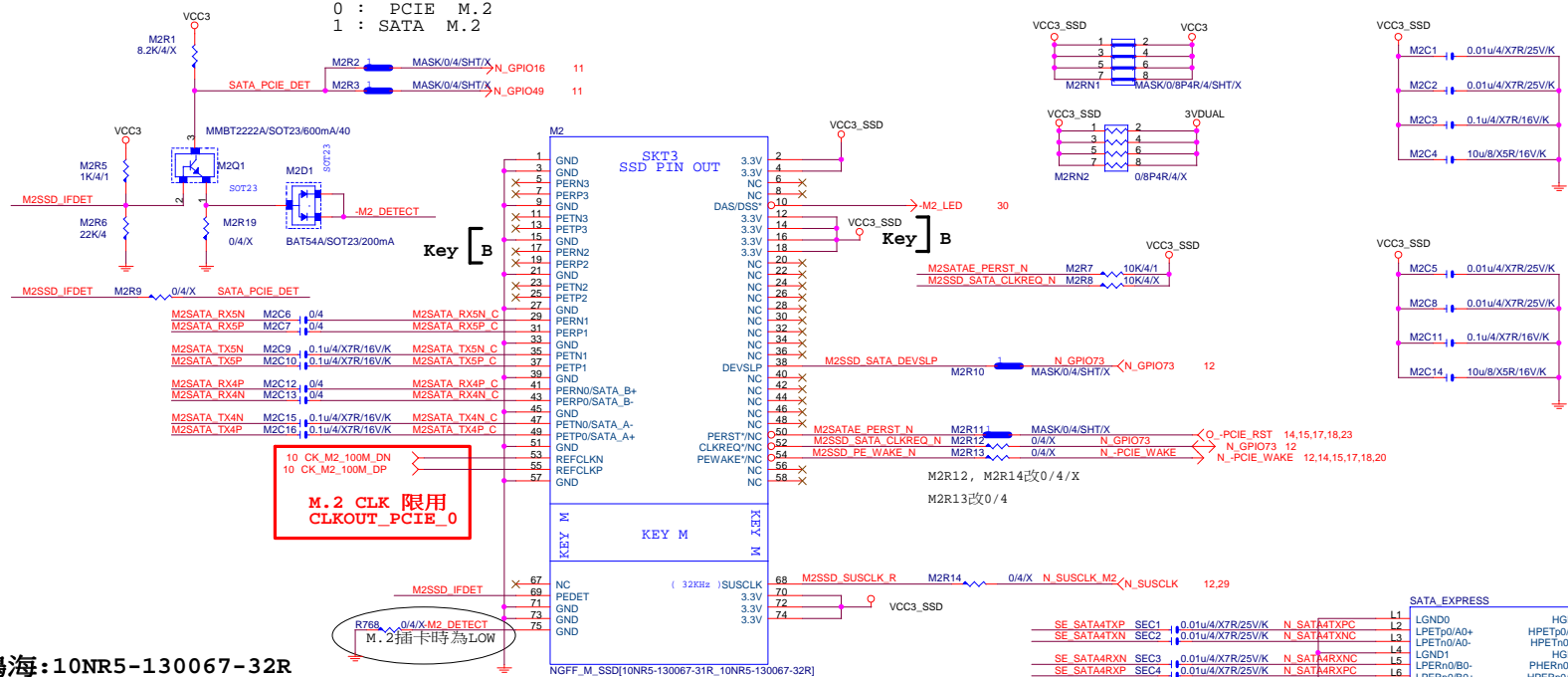
USB3.0 1Port - 1Fuse (3.5A)

USB20 ESD PROTECT



Title			
HDMI			
Size	Document Number	Rev	
Custom	Z97X-UD3H	1.0	
Date:	Tuesday, April 08, 2014	Sheet	34 of 37

0 : PCIE M.2
1 : SATA M.2



M.2 CLK 限用
CLKOUT_PCIE_0

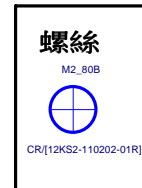
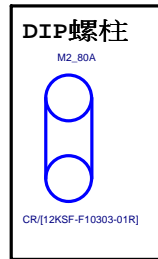
M.2 插卡時為LOW

PCH

SATA EXPRESS

M2

Function	SEL
xI--> x0a	L
xI--> x0b	H



SATA EXPRESS料號

單層:11NR6-C10118-01R

雙層:11NR6-C10236-01R

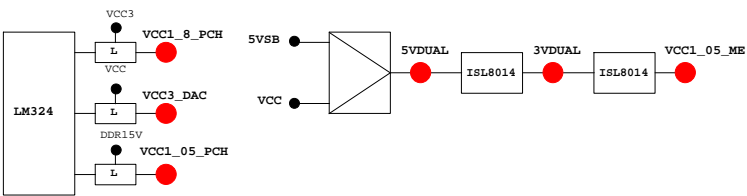
GIGABYTE™		
M2 SATA EXPRESS		
Title	Document Number	Rev
Size	Custom	297X-UD3H
Date:	Tuesday, April 08, 2014	Sheet 36 of 37

PCH GPIO LIST TABLE					
PIN NAME	PWR	Default	USAGE	NOTE	
GP0	MAIN	H-Z	GPI	GPIO0	N/A
GP1/TACH1	MAIN		GPI	GPIO1	N/A
GP2/PIRQE#	MAIN		GPI	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN		GPI	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN		GPI	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN		GPI	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN		GPI	PCIEX1 Detect	P/U 8.2K VCC3
GP7/TACH3	MAIN		GPI	GPIO7	P/U 8.2K VCC3
GP8	STBY	H	GPI	GPIO8	N/A
GP9/OC5#	STBY		NATIVE	USB OC5#	N/A
GP10/OC6#	STBY		NATIVE	USB OC6#	N/A
GP11/SMBALERT#	STBY		NATIVE	USB PWR protect	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI	GPIO12	N/A
GP13	STBY	L	GPI	LPCPME#	P/U 8.2K 3VDUAL
GP14/OC7#	STBY		NATIVE	USB OC7#	N/A
GP15	STBY	L	GPI	GPIO15(TLS Enable)	P/U 8.2K 3VDUAL
GP16	MAIN		GPI	GPIO16	P/U 8.2K VCC3
GP17/TACH0	MAIN		GPI	GPIO17	P/U 8.2K VCC3
GP18	MAIN		GPI	Mobile Only	N/A
GP19	MAIN		GPI	GPIO19	P/U 8.2K VCC3
GP20	MAIN		GPI	GPIO20	P/U 8.2K VCC3
GP21	MAIN		GPI	GPIO21	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI	GPIO22	P/U 8.2K VCC3
GP23	MAIN		GPI	GPIO23	N/A
GP24	STBY	L	GPI	SKTOCC#	N/A
GP25	STBY			Mobile Only	N/A
GP26	STBY			Mobile Only	N/A
GP27	STBY	H	GPO	GPIO27	P/U 8.2K 3VDUAL
GP28	STBY	H	GPO	PWR LED	P/U 8.2K 3VDUAL
GP29	STBY	L	GPI	GPIO29	N/A
GP30	STBY	H-Z	GPI	Mobile Only	N/A
GP31	STBY	H-Z	GPI	Mobile Only	N/A
GP32	MAIN	H	GPO	N/A	N/A
GP33	MAIN	H	GPO	N/A	N/A
GP34	MAIN	H-Z	GPI	-PCI_STOP	P/U 8.2K VCC3
GP35	MAIN	L	GPO	-ACZ_DET	P/U 8.2K VCC3
GP36	MAIN		GPI	N/A	N/A
GP37	MAIN		GPI	N/A	N/A
GP38	MAIN	H-Z	GPI	PCIEX4 Detect	P/U 8.2K VCC3
GP39	MAIN	H-Z	GPI	GPIO39	P/U 8.2K VCC3
GP40	STBY		NATIVE	USB OC1#	N/A
GP41	STBY		NATIVE	USB OC2#	N/A
GP42	STBY		NATIVE	USB OC3#	N/A
GP43	STBY		NATIVE	USB OC4#	N/A
GP44	STBY	L	NATIVE	GPIO44	P/U 8.2K 3VDUAL
GP45	STBY		NATIVE	GPIO45	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE	GPIO46	P/U 8.2K 3VDUAL
GP47	STBY			Mobile Only	N/A
GP48	MAIN	H-Z	IN	GPIO48	P/U 8.2K 3VDUAL
GP49	MAIN	H-Z	IN	GPIO49	P/U 8.2K 3VDUAL
GP50	MAIN		NATIVE	-REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE	-GNT1	N/A
GP52	MAIN		NATIVE	-REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE	-GNT2	N/A
GP54	MAIN		NATIVE	-REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE	-GNT3	N/A
GP56	STBY		NATIVE	Mobile Only	N/A
GP57	STBY	H-Z	IN	VCORE_OV1	P/U 8.2K 3VDUAL
GP58	STBY	H-Z	NATIVE	F_USB_OC	P/U 8.2K 3VDUAL
GP59	STBY		NATIVE	USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP61	STBY	L	NATIVE	-SUSTAT	N/A
GP62	STBY	L	NATIVE	SUSCLK	N/A
GP63	STBY	L	NATIVE	GPIO63	N/A
GP64	MAIN	L	NATIVE	CLKOUTFLEX0	N/A
GP65	MAIN	L	NATIVE	CLKOUTFLEX1	N/A
GP66	MAIN	L	NATIVE	CLKOUTFLEX2	N/A
GP67	MAIN	L	NATIVE	CLKOUTFLEX3	N/A
GP72	STBY	H-Z	NATIVE	VCORE_OV4	P/U 8.2K 3VDUAL
GP73	STBY			Mobile Only	N/A
GP74	STBY	H-Z	NATIVE	1_05V_OV2	P/U 8.2K 3VDUAL
GP75	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL

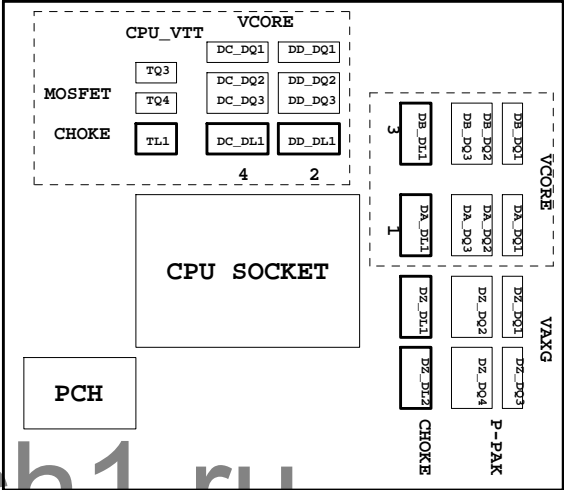
Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCI_E_RST	
RSMRST#CIRRXL/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSS00	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSSI1	SB_LED1_C	
PD4/GP74/BUSSI2	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSSI0	NB_LED3_C	
GP22/SCK	LOW_PWR_1	
VID05/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PWRST1	
PCIRST1#/GP12	-PWRST2	
3VBSBW#/GP40	CSI_F0	BSEL166_1
SUSC#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VID00/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSS01	MB_ID3	
PD7/GP77/BUSS02	MB_ID4	
AFD#/GP86/SMBC_R	SEC_PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VID01/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMBC_M	DDR_LED3_C	
PWRON#/GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRXL2/GP16	-THERM	
VID04/GP26/SOUT2	DDR18V_PH2_EN	
VID02/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VID06/GP17/RI2#	1_1V_PH_EN	
VID07/JP6/DTR2#	JP6	
PD5/GP75/BUSS00	SB_LED3_C	



PWM各相位的擺法如下：



BIOS超電壓對應表：

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Terminatio
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

散熱模組料號：

Z77-D3H :
PCH :
12SP2-S05511-01R/02R/03R
MOSFET :
12SP2-S08924-01R/02R/03R

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH